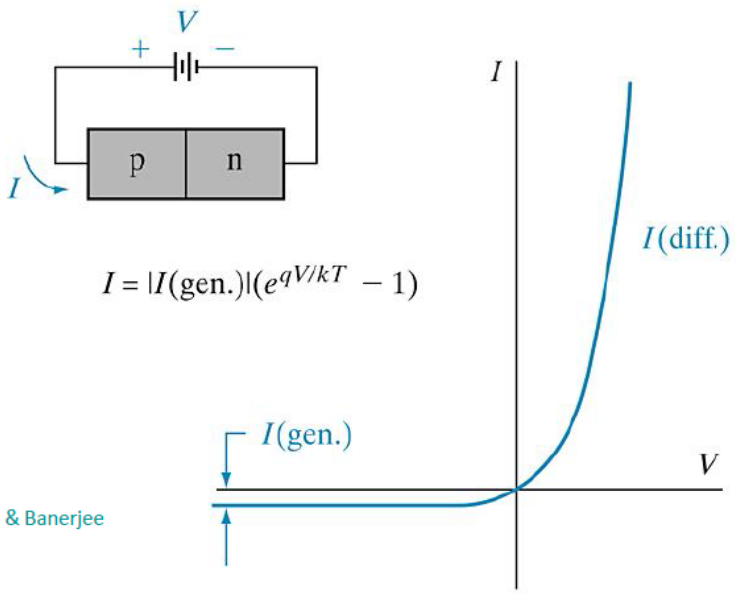
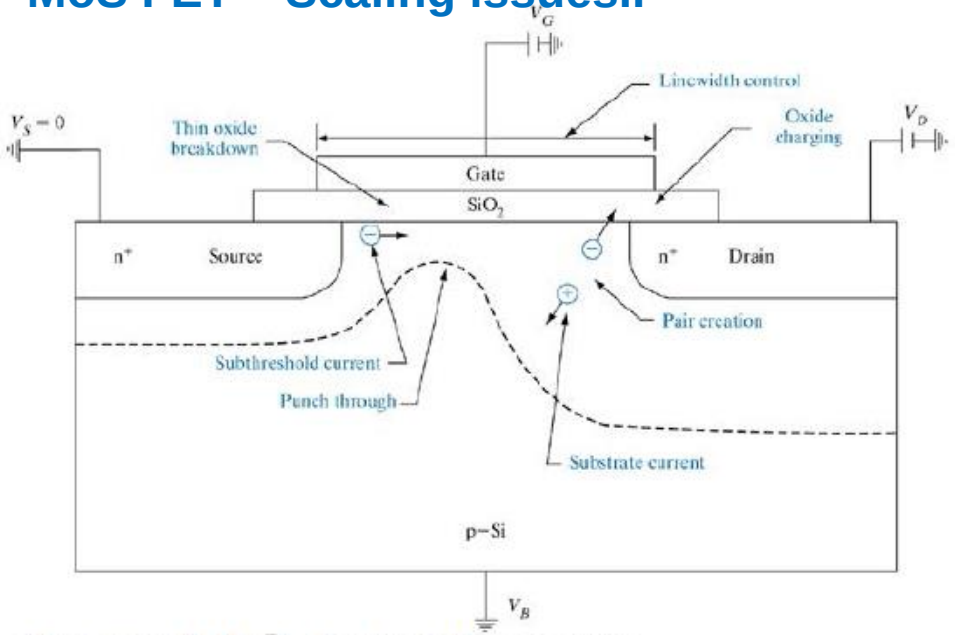
PN Diode, Transistors – MOS FET …and C-MOS

The p-n diode



- **Forward-bias: large current due to minority carrier diffusion**
- **Reverse bias: small current due to minority carrier generation and drift**

MoS FET – Scaling issues..

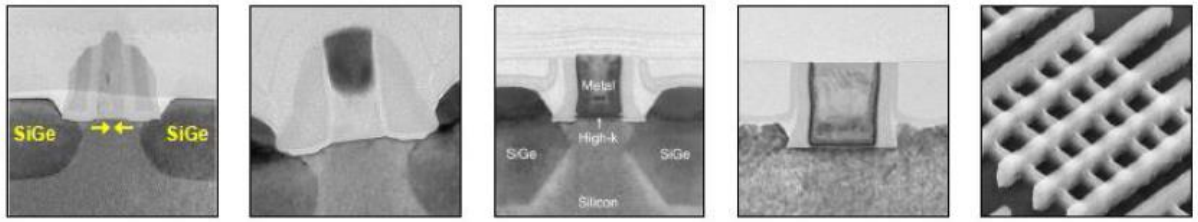


- **Constant field ➔ electrostatic integrity**
- **Constant voltage ➔ noise immunity**
- **Scaled devices prone to short-channel effects, including**
  - Breakdown of thin gate oxide
  - Hot-carrier generation
  - Punchthrough breakdown between source/drain

C-MOS architecture dominates semiconductor industry …high noise immunity / low power consumptions

New Materials & Device Structures…

2003	2005	2007	2009	2011
90 nm	65 nm	45 nm	32 nm	22 nm



Strained channel

➔ higher carrier speed

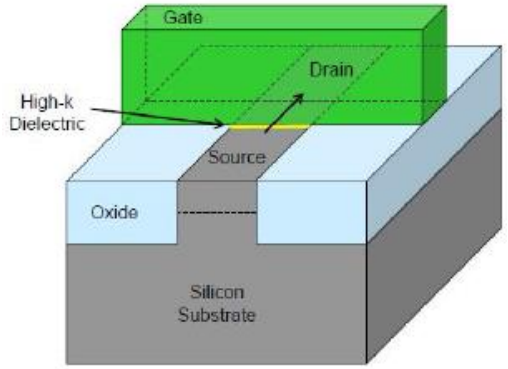
High-k, metal gate stack ➔

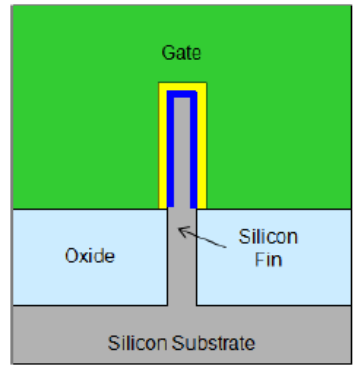
lower gate leakage

Multi-gate, thin body

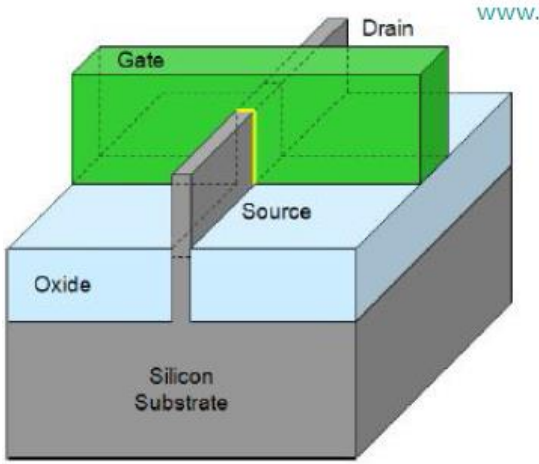
➔ better electrostatics

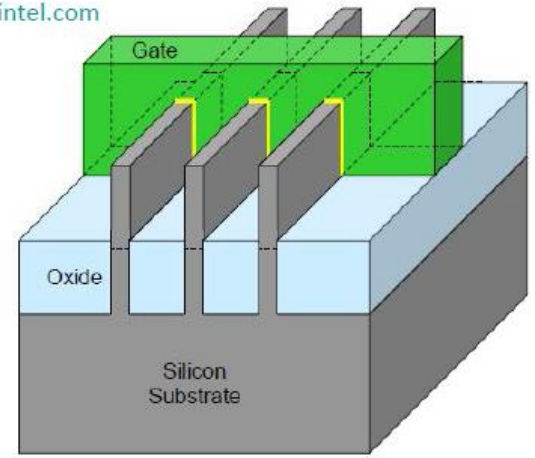
➔ more scalable



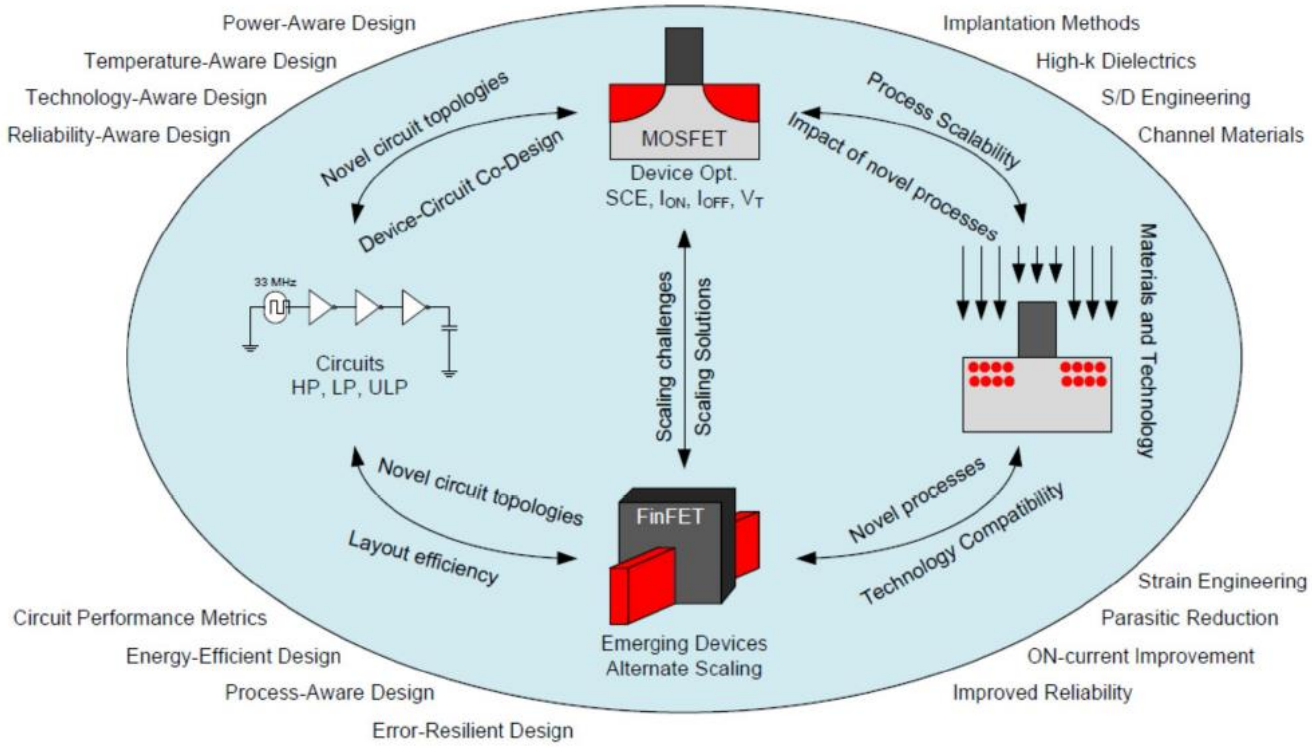


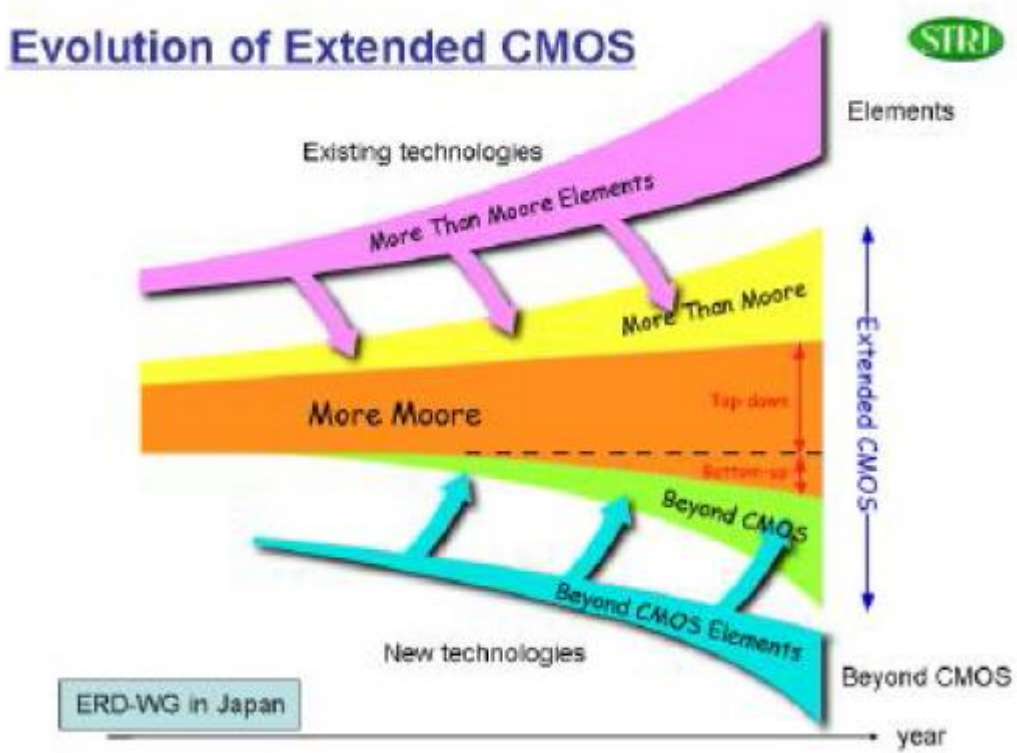
www.intel.com





CMOS Scaling today…and tomorrow…



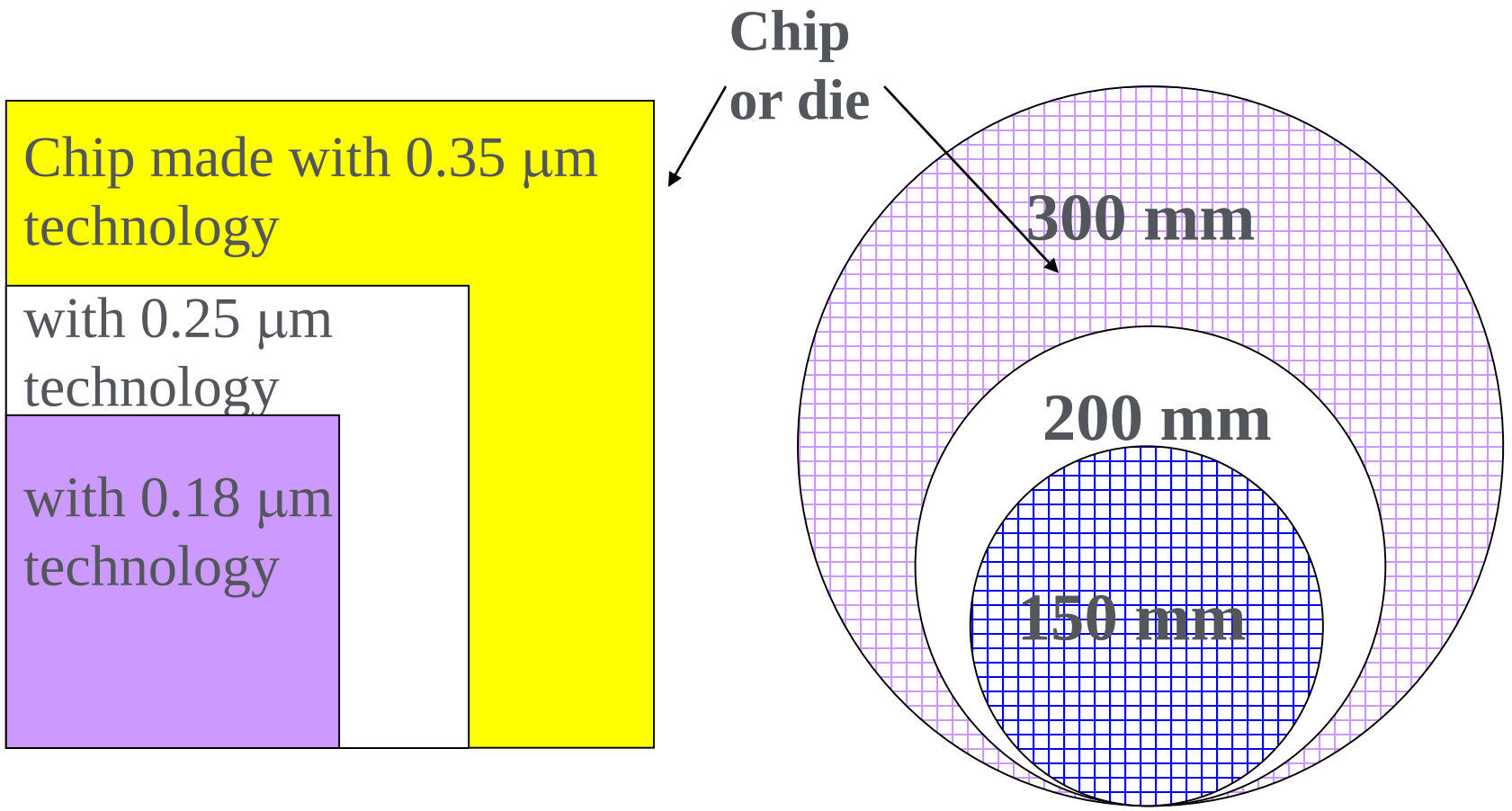


More-of-Moore: Dimensional & Functional Scaling
More-than Moore: Heterogenous Integration, Sensors, Energy harvesting…
Beyond CMOS: Spintronics (MeRAM); NeuroMorphic…

Semiconductor Manufacturing

Manufacturing Process
Semiconductor Equipment
The Fab (possible layout, cleanroom concepts, subfab & related concepts)

Feature Size and Wafer Size



www2.austin.cc.tx.us/HongXiao/Book.htm Hong Xiao, Ph.

Cleanroom Environments

APPLIED MATERIALS® make possible

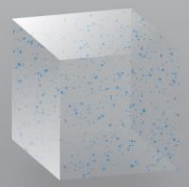
Why does a chip have to be made in a cleanroom?

The dimensions of the critical structures and circuitry on a chip are so tiny – measuring in nanometers (one billionth of a meter) that particles or dust, like pollen, in the air can damage them.

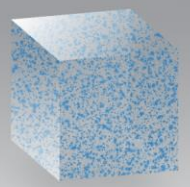
How clean is your room?

Cleanrooms are classed by the number of particles per cubic foot of air. Semiconductor cleanrooms are 3 million times cleaner than outside air.

CLASS 1
Cleanroom with no more than 1 particle (≥5 micron size) per cubic foot of air

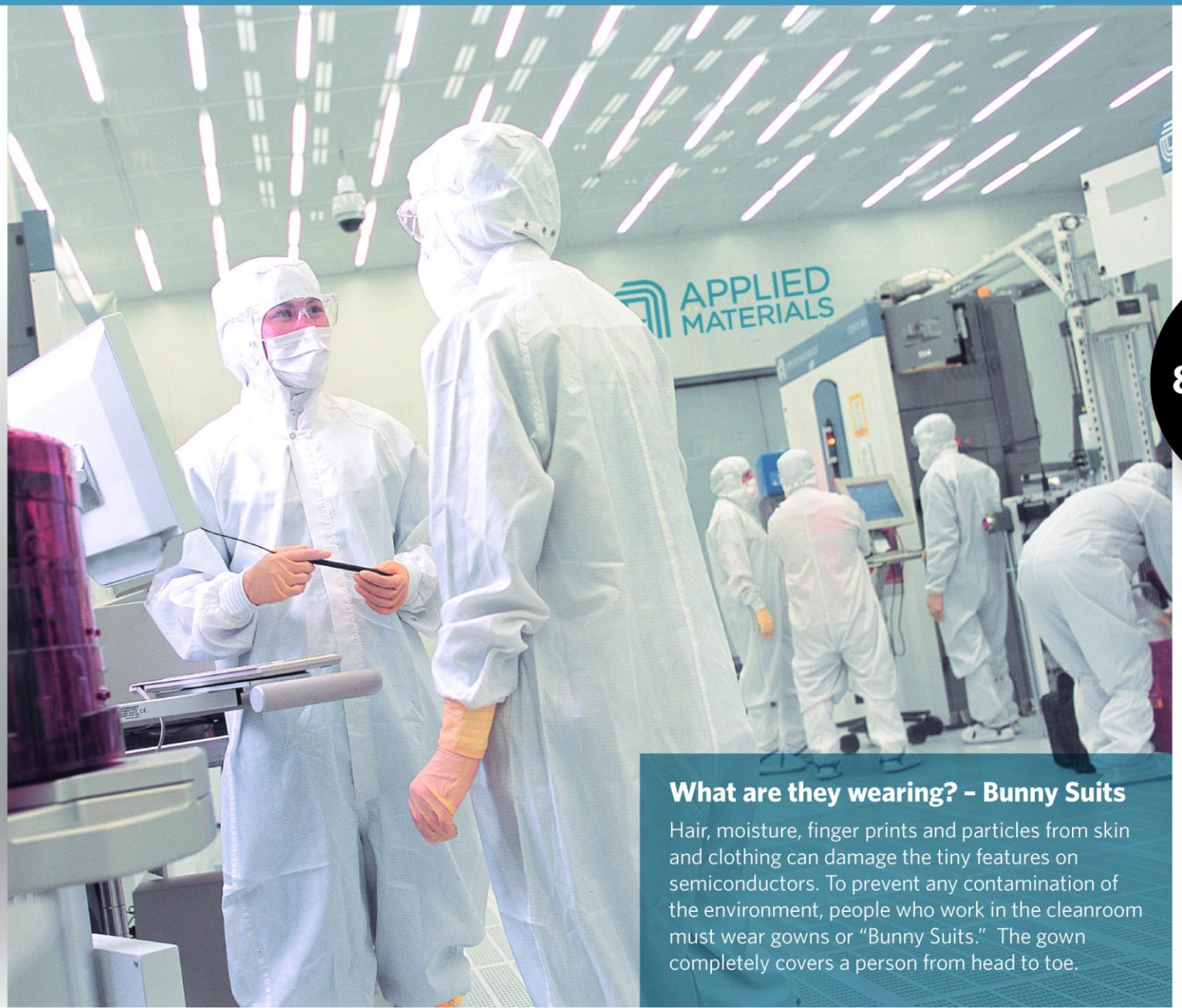


CLASS 10,000
Hospital operating room with no more than 10,000 particles per cubic foot of air



CLASS 3 MILLION
Outside air has approximately 3 million particles per cubic foot of air

*Federal Standard 209E

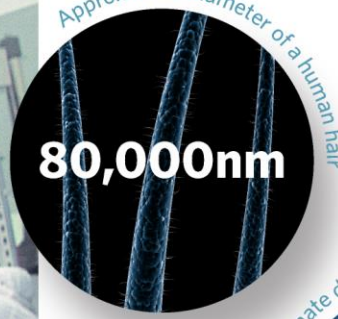


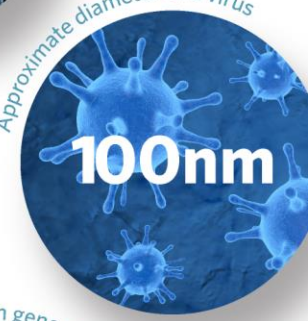
What are they wearing? – Bunny Suits

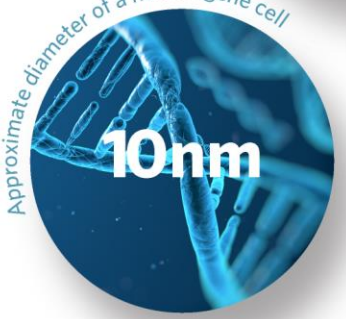
Hair, moisture, finger prints and particles from skin and clothing can damage the tiny features on semiconductors. To prevent any contamination of the environment, people who work in the cleanroom must wear gowns or "Bunny Suits." The gown completely covers a person from head to toe.

How small is a nanometer?

A nanometer (nm) is one billionth of a meter. If a feature on a chip measures 10nm, then about 8,000 of those features can fit across the width of a single human hair.





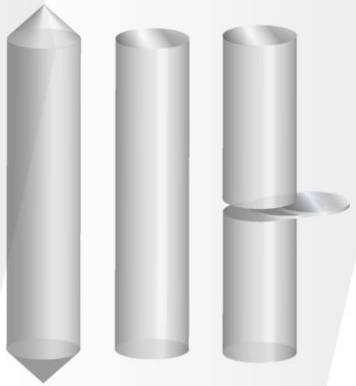


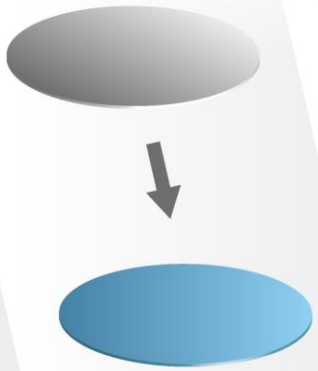
How to Make a Chip

FROM SAND TO WAFER

Silicon, the second most common element on Earth, is refined from sand into pure silicon dioxide, and then melted and pulled to form a cylinder called a crystal ingot.

The ingot is polished and then sliced into thin wafers – typically 300mm or 12 inches in diameter.





WAFER PREP

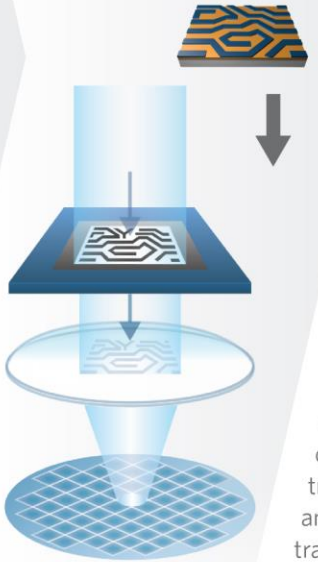
A pure layer of silicon is grown on the wafer surface using a process called Epi to protect the underlying silicon during subsequent steps.

Next, the wafer is spun and uniformly coated with a thick light-sensitive liquid called photoresist.

PATTERN FORMATION

Circuit patterns are drawn on a clear stencil-like mask, and transferred to the photoresist using ultraviolet light.

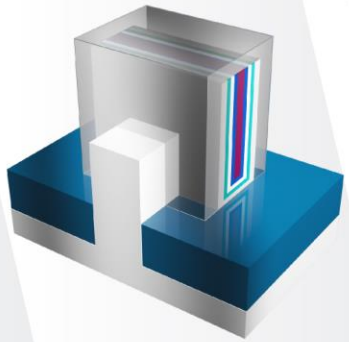
Materials in unexposed areas are etched away, leaving a 3D pattern on the wafer. These steps repeat multiple times and require precise measurement.



TRANSISTOR FORMATION

The transistor is the fundamental building block of electronics. It is a switch or gate that regulates voltage. Advanced chips can contain 12 billion transistors.

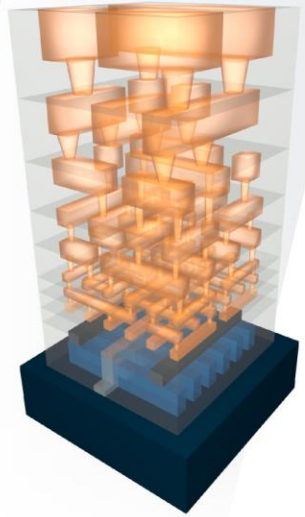
Switching a gate open allows current to flow through a channel from a source to a drain. Etch and deposition steps form the transistor. Ion implantation and thermal steps improve transistor speed by modifying the silicon to conduct current faster.

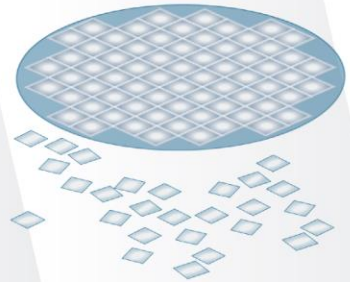


CONNECT TRANSISTORS

Wires connect transistors to route electronic signals out of the chip, and are created by patterning and etching circuit lines, then filling them with metal.

A single chip can contain more than 12.5 miles of wiring spanning multiple levels.



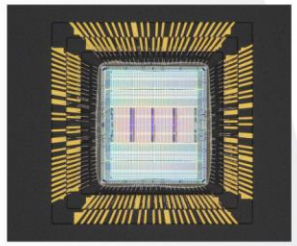


CUT INTO SINGLE CHIPS

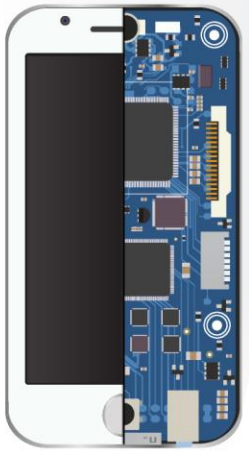
When the wafer is finished being processed, the surface is now covered with multiple semiconductors. The wafer is sliced into individual semiconductor "chips."

PACKAGING

The chips are then placed in a lead frame forming a protective housing.



Each chip is tested before being packaged. They are now ready to be used in computers, mobile devices and many other products.



Device Fabrication Technology

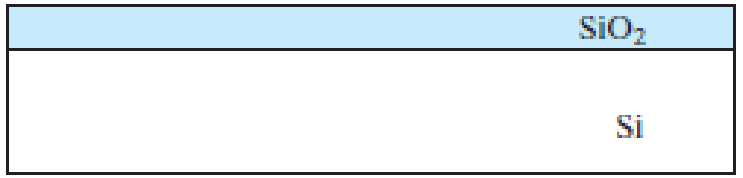
About 10^{20} transistors (or 10 billion for every person in the world) are manufactured every year.

VLSI (Very Large Scale Integration)
ULSI (Ultra Large Scale Integration)
GSI (Giga-Scale Integration)

Variations of this versatile technology are used for flat-panel displays, micro-electro-mechanical systems (***MEMS***), and chips for DNA screening...

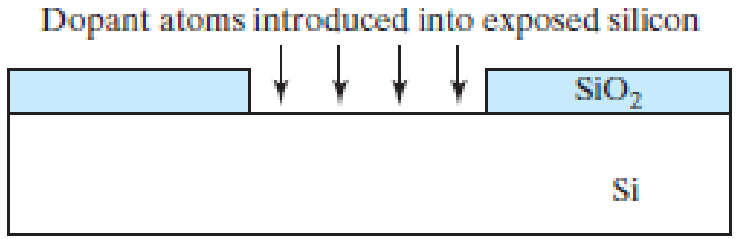
3.1 Introduction to Device Fabrication

Oxidation

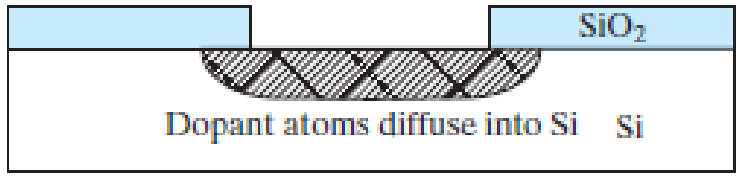


Lithography & Etching

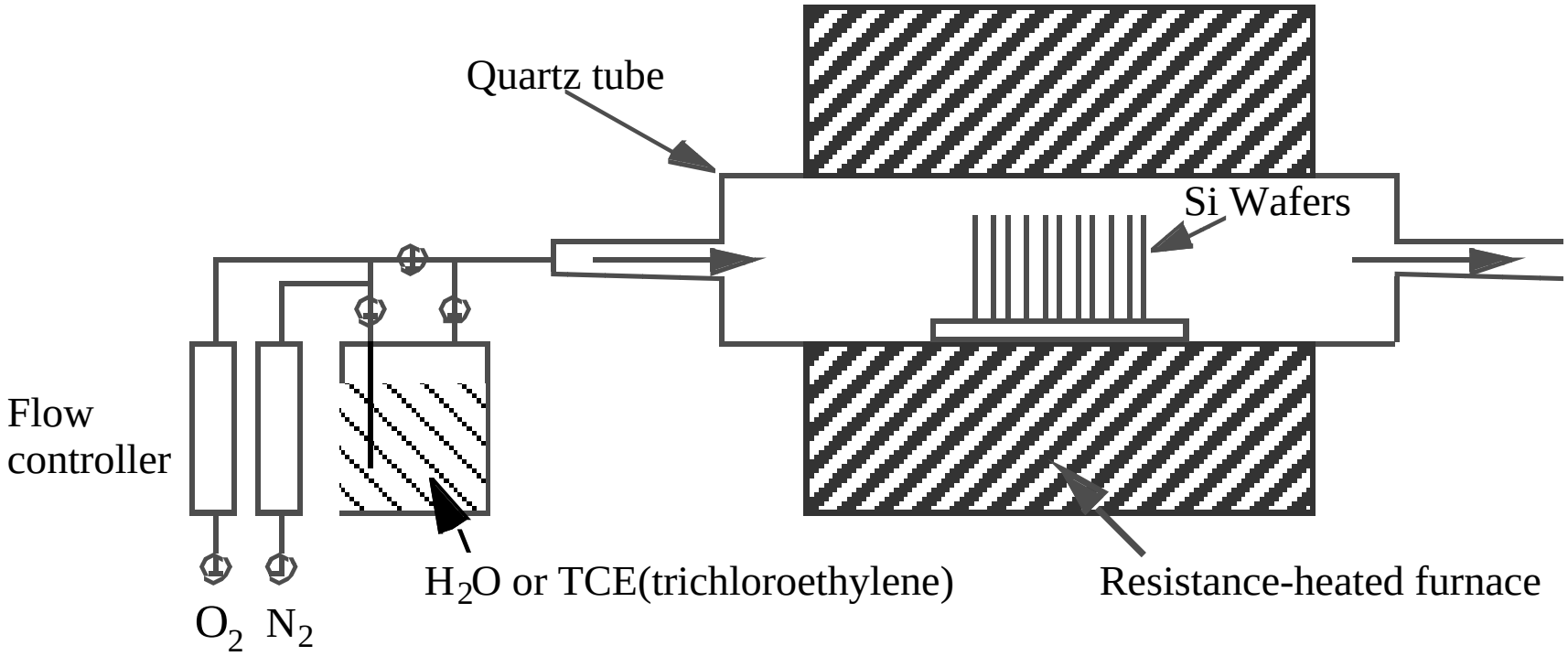
Ion Implantation



Annealing & Diffusion



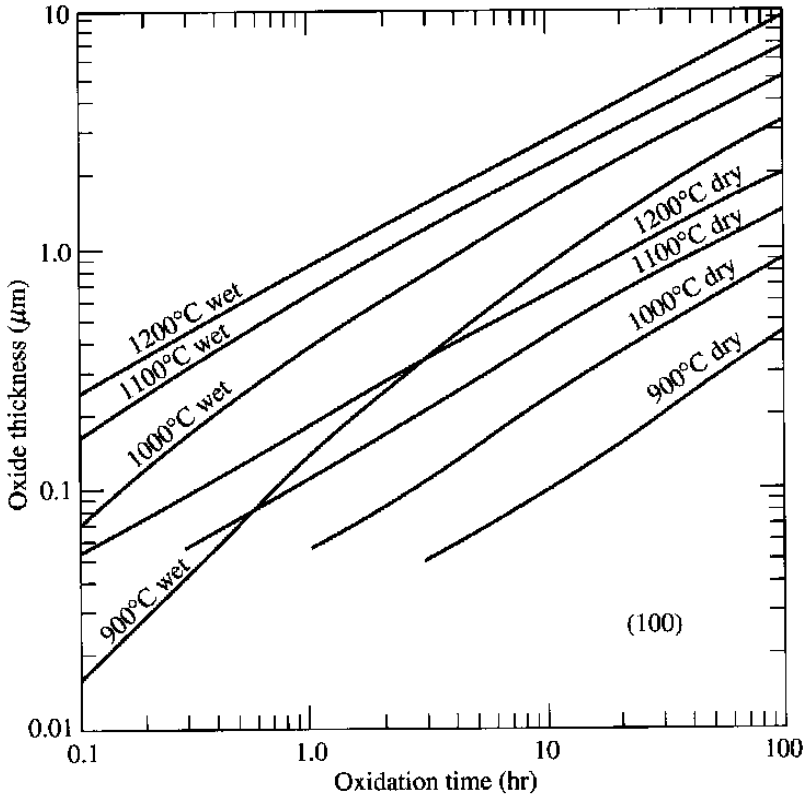
3.2 Oxidation of Silicon



3.2 Oxidation of Silicon

Dry Oxidation : $Si + O_2 \rightarrow SiO_2$

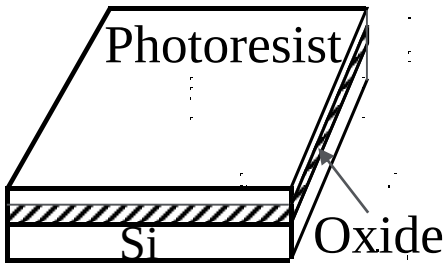
Wet Oxidation : $Si + 2H_2O \rightarrow SiO_2 + 2H_2$



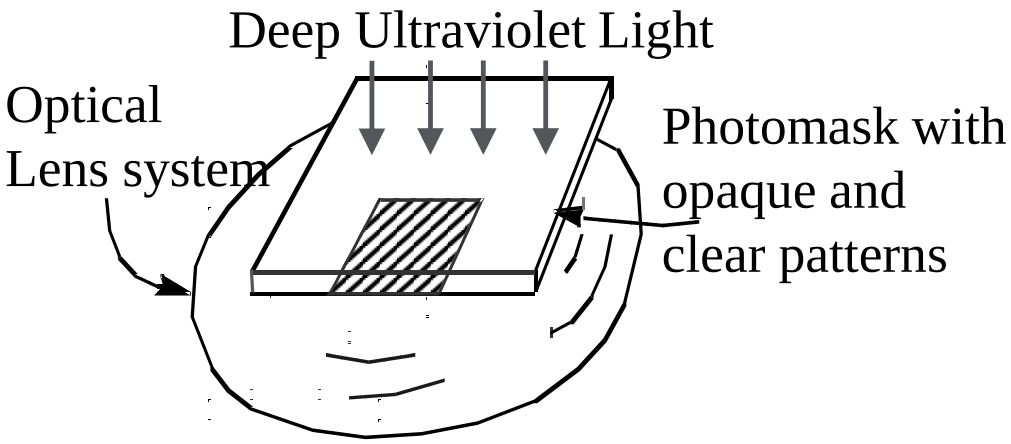
Modern Semiconductor Devices for Integrated Circuits (C. Hu)

3.3 Lithography

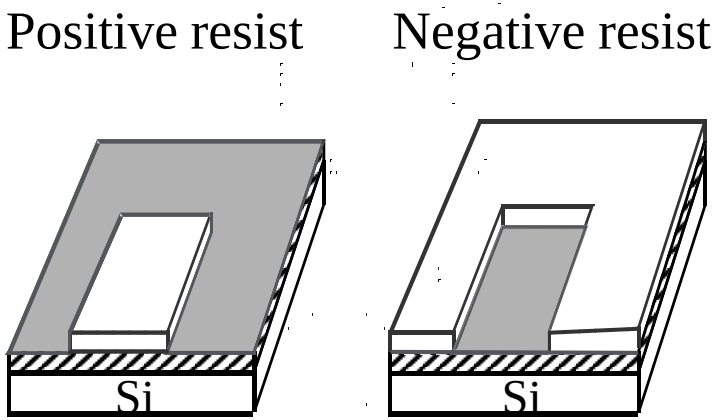
(a) Resist Coating



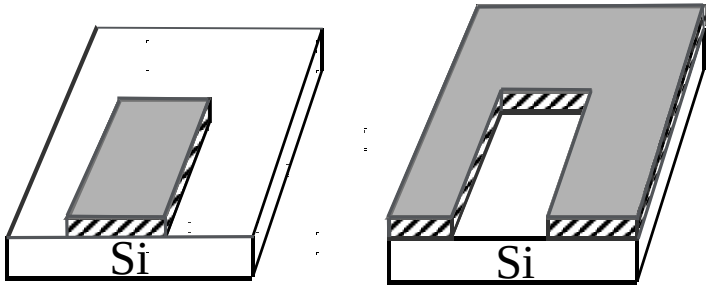
(b) Exposure



(c) Development



(d) Etching and Resist Strip



3.3 Lithography

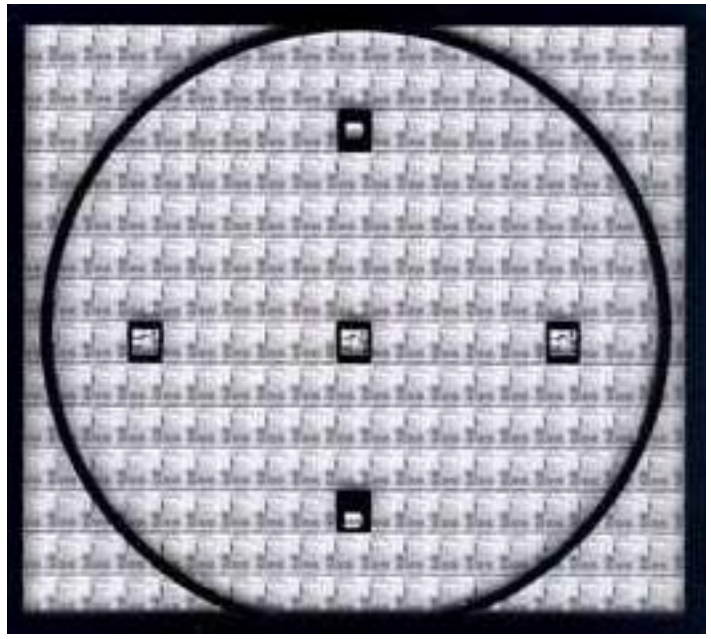
Photolithography Resolution Limit, *R*

- $R \geq k\lambda$ due to optical diffraction
- Wavelength λ needs to be minimized. (248 nm, 193 nm, 157 nm?)
- k (<1) can be reduced with
  - Large aperture, high quality lens
  - Small exposure field, step-and-repeat using “stepper”
  - Optical proximity correction
  - Phase-shift mask, etc.
- Lithography is difficult and expensive. There can be 40 lithography steps in an IC process.

3.3 Lithography

Wafers are being loaded into a stepper in a clean room.

A Mask and a Reticle



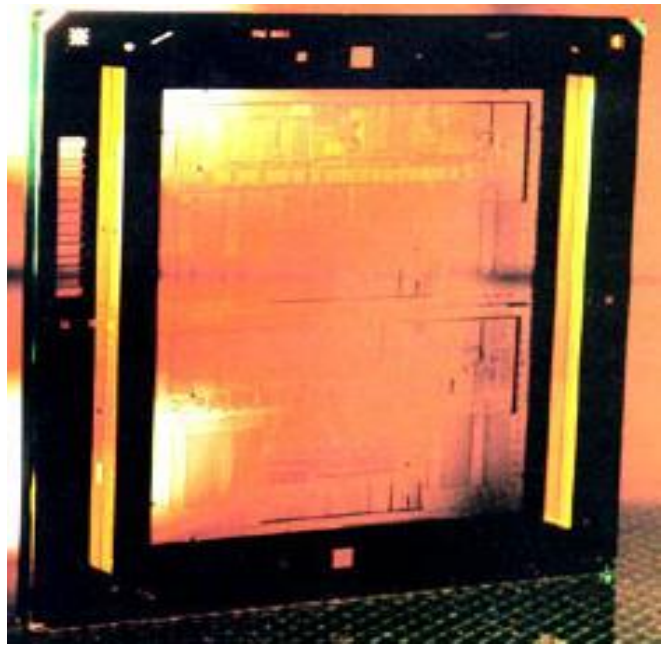
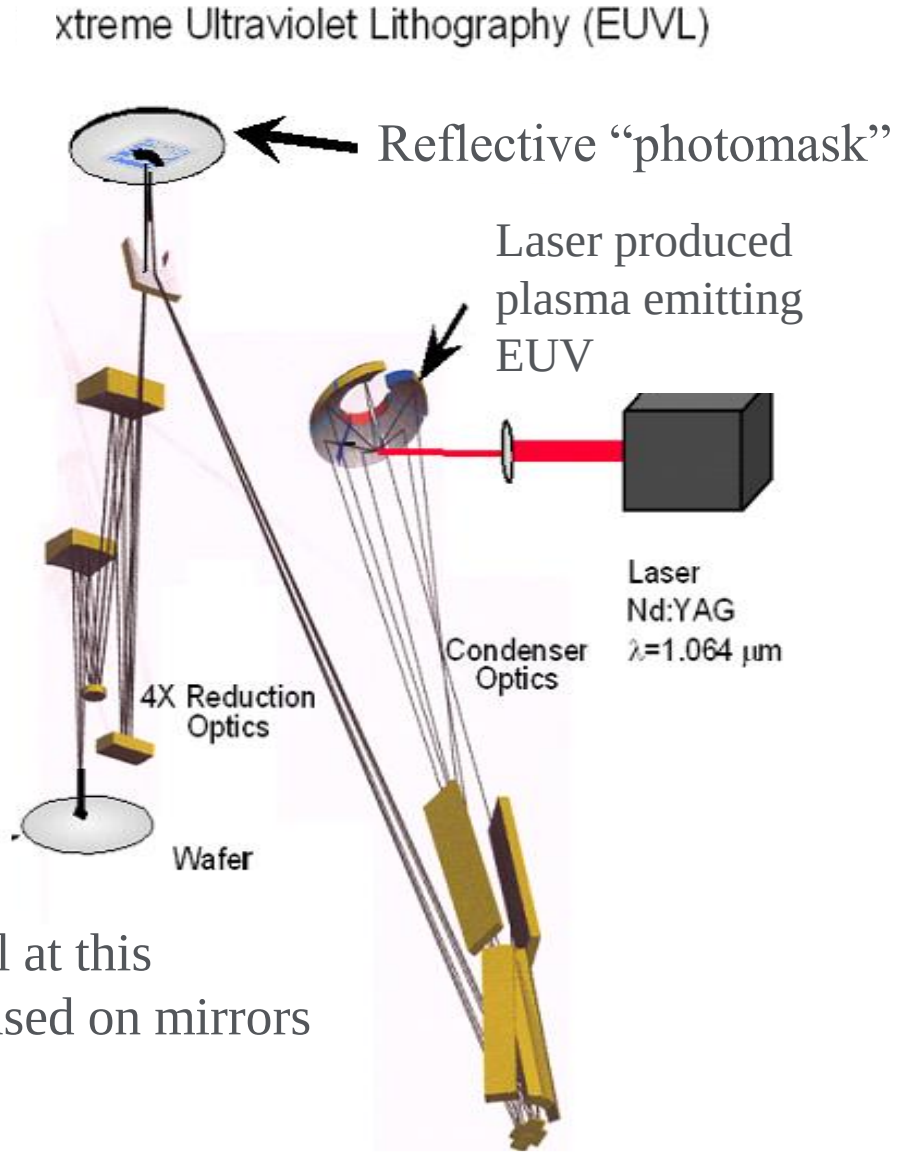


Photo courtesy: SGS Thompson

www2.austin.cc.tx.us/HongXiao/Book.htm Hong Xiao, Ph.

Extreme UV Lithography (13nm wavelength)



No suitable lens material at this wavelength. Optics is based on mirrors with nm flatness.

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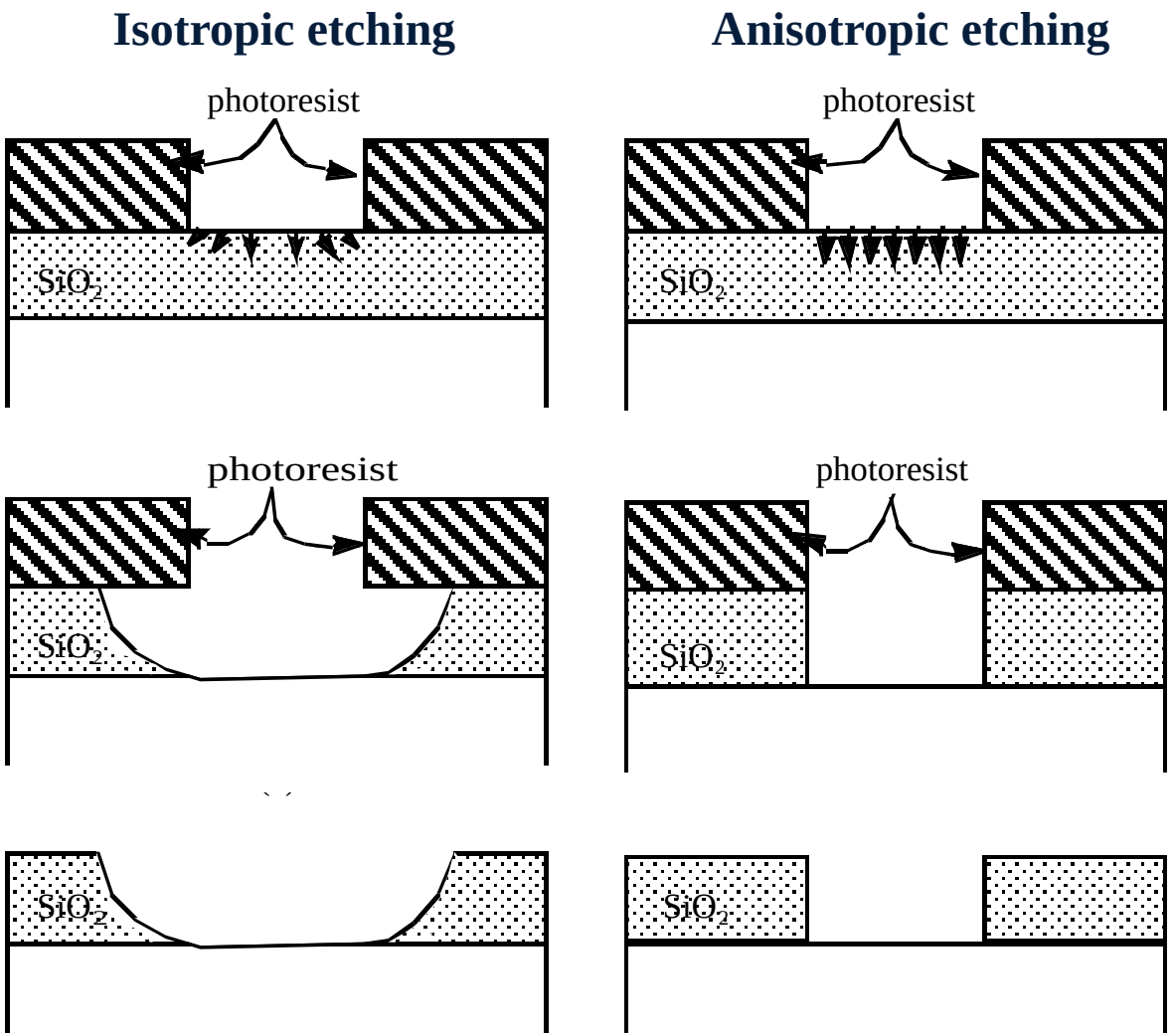
Beyond Optical Lithography

- ***Electron Beam Writing*** : Electron beam(s) scans and exposed electron resist on wafer. Ready technology with relatively low throughput.

- ***Electron Projection Lithography*** : Exposes a complex pattern using mask and electron lens similar to optical lithography.

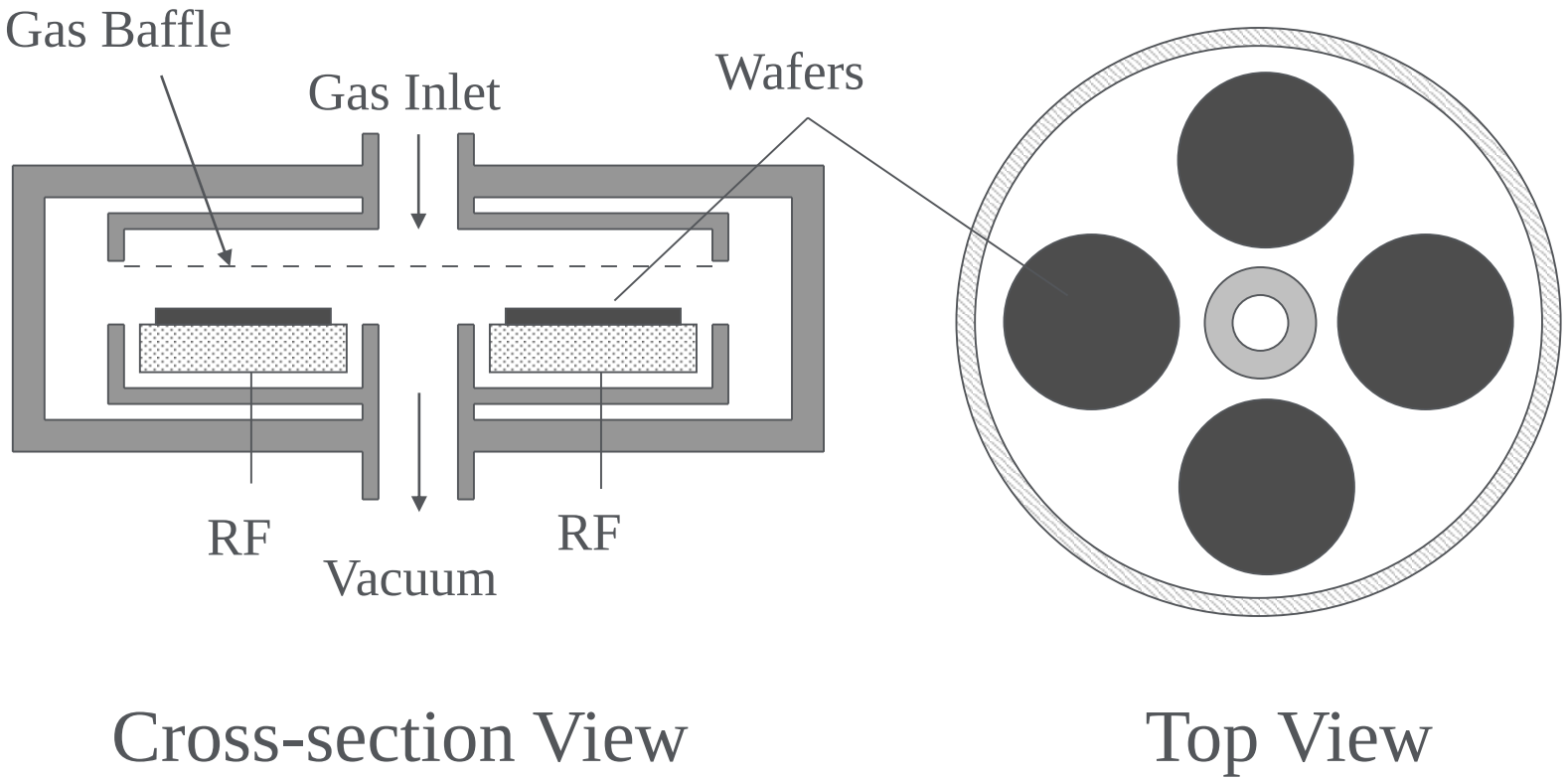
- ***Nano-imprint*** : Patterns are etched into a durable material to make a "stamp." This stamp is pressed into a liquid film over the wafer surface. Liquid is hardened with UV to create an imprint of the fine patterns.

3.4 Pattern Transfer–Etching



3.4 Pattern Transfer–Etching

Reactive-Ion Etching Systems

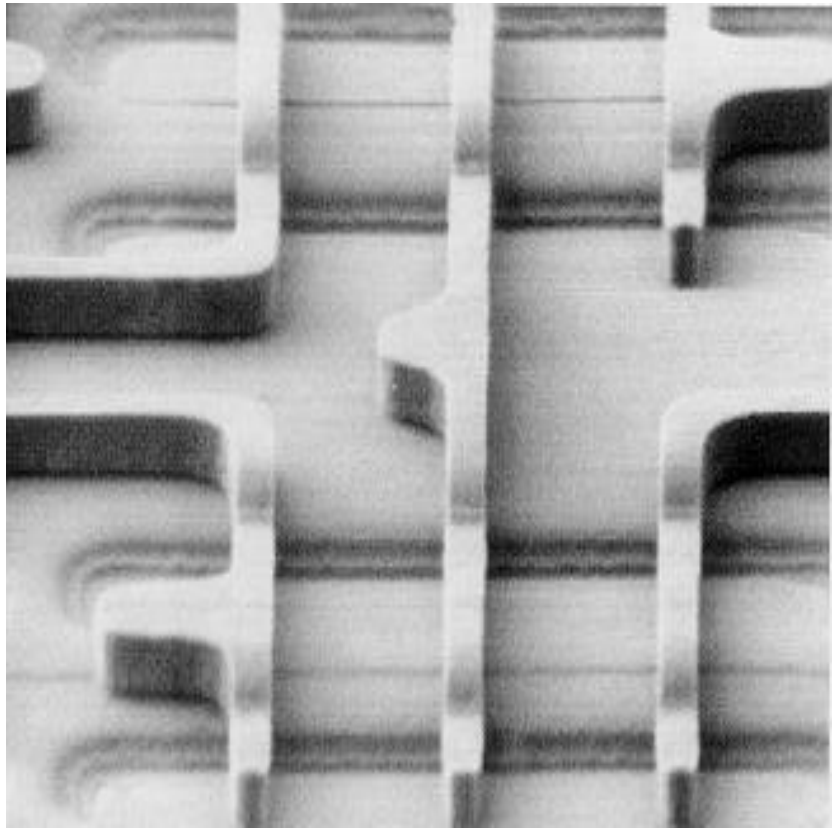


3.4 Pattern Transfer–Etching

Dry Etching (also known as Plasma Etching, or Reactive-Ion Etching) is anisotropic.

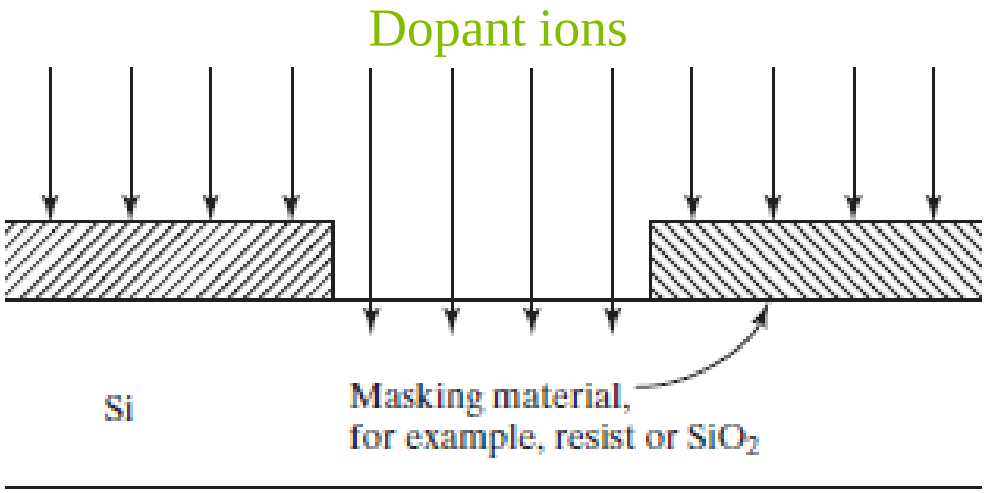
- Silicon and its compounds can be etched by plasmas containing F.
- Aluminum can be etched by Cl.
- Some concerns :
  - Selectivity and End-Point Detection
  - Plasma Process-Induced Damage or Wafer Charging Damage and Antenna Effect

Scanning electron microscope view of a plasma-etched 0.16 μm pattern in polycrystalline silicon film.



3.5 Doping

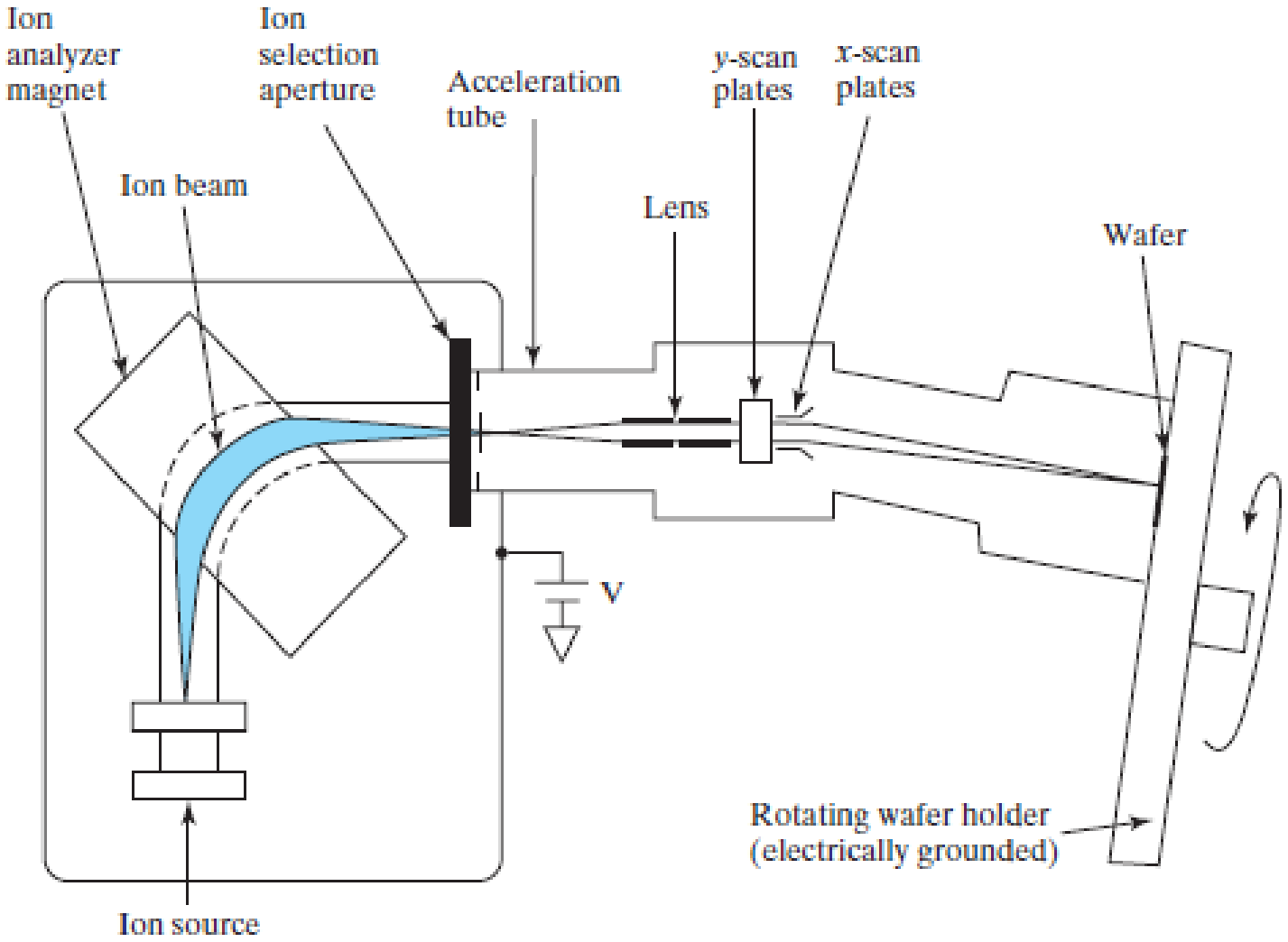
3.5.1 Ion Implantation



- The dominant doping method
- Excellent control of **dose** (cm^{-2})
- Good control of implant depth with energy (KeV to MeV)
- Repairing crystal damage and dopant activation requires annealing, which can cause dopant diffusion and loss of depth control.

3.5.1 Ion Implantation

Schematic of an Ion Implanter



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3.5.1 Ion Implantation

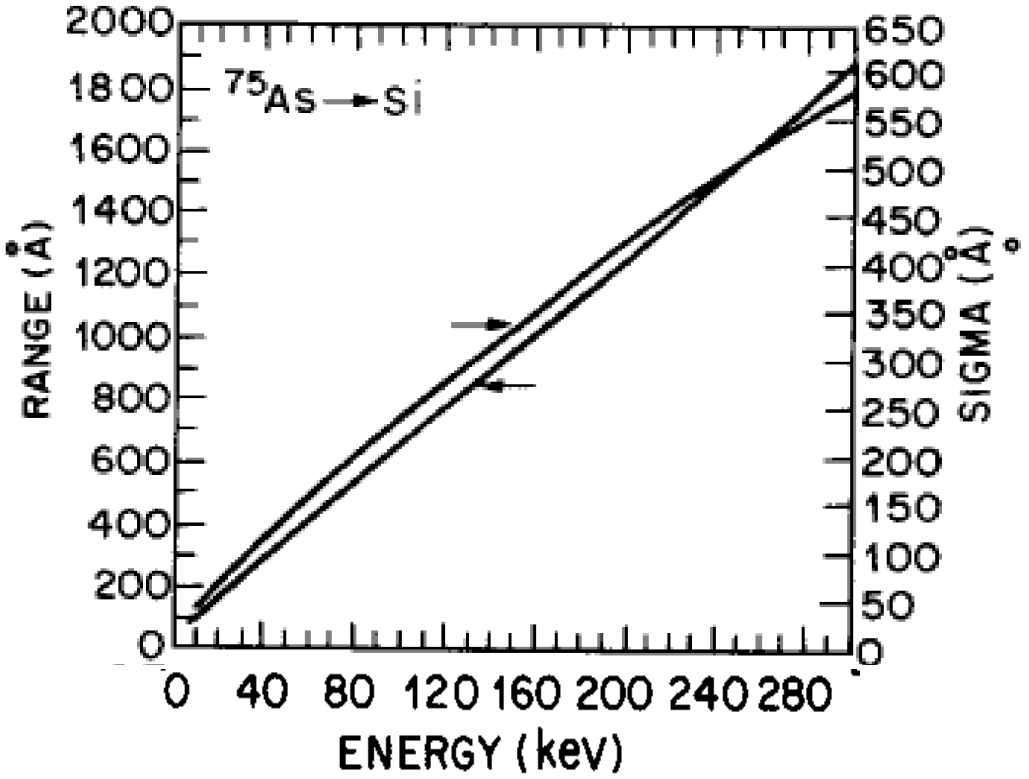
Model of Implantation Doping Profile (Gaussian)

$$N(x) = \frac{N_i}{\sqrt{2\pi} \cdot (\Delta R)} \cdot e^{-(x-R)^2 / 2\Delta R^2}$$

N_i : dose (cm^{-2})

R : range or depth

ΔR : spread or sigma



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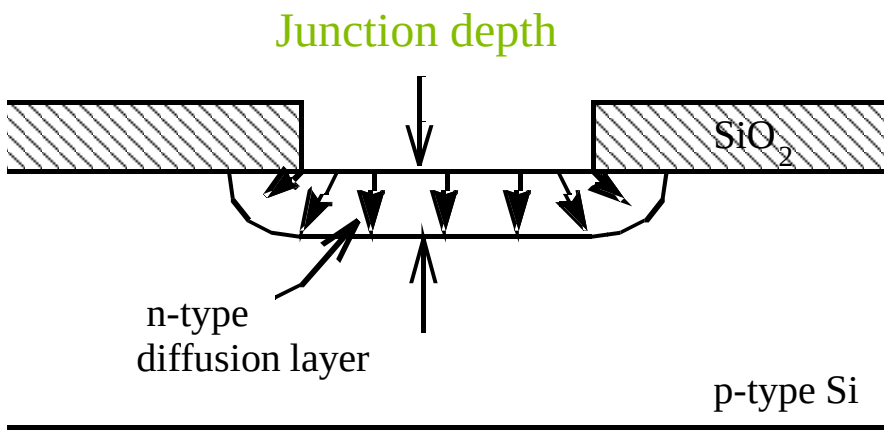
Other Doping Methods

- ***Gas-Source Doping*** : For example, dope Si with P using $POCl_3$.
- ***Solid-Source Doping*** : Dopant diffuses from a doped solid film (SiGe or oxide) into Si.
- ***In-Situ Doping*** : Dopant is introduced while a Si film is being deposited.

3.6 Dopant Diffusion



$$N(x,t) = \frac{N_o}{\sqrt{\pi \cdot Dt}} e^{-x^2/4Dt}$$

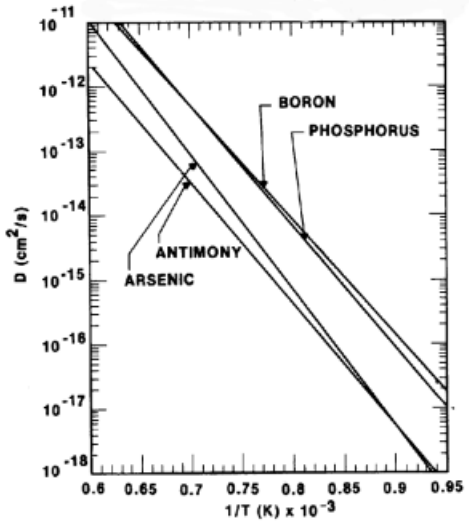
N : N_d or N_a (cm^{-3})

N_o : dopant atoms per cm^2

t : diffusion time

D : diffusivity, $\sqrt{Dt}$ is the approximate distance of dopant diffusion

3.6 Dopant Diffusion



- D increases with increasing temperature.
- Some applications need very deep junctions (high T, long t). Others need very shallow junctions (low T, short t).

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Modern Semiconductor Devices for Integrated Circuits (C. Hu)

3.6 Dopant Diffusion

Shallow Junction and Rapid Thermal Annealing

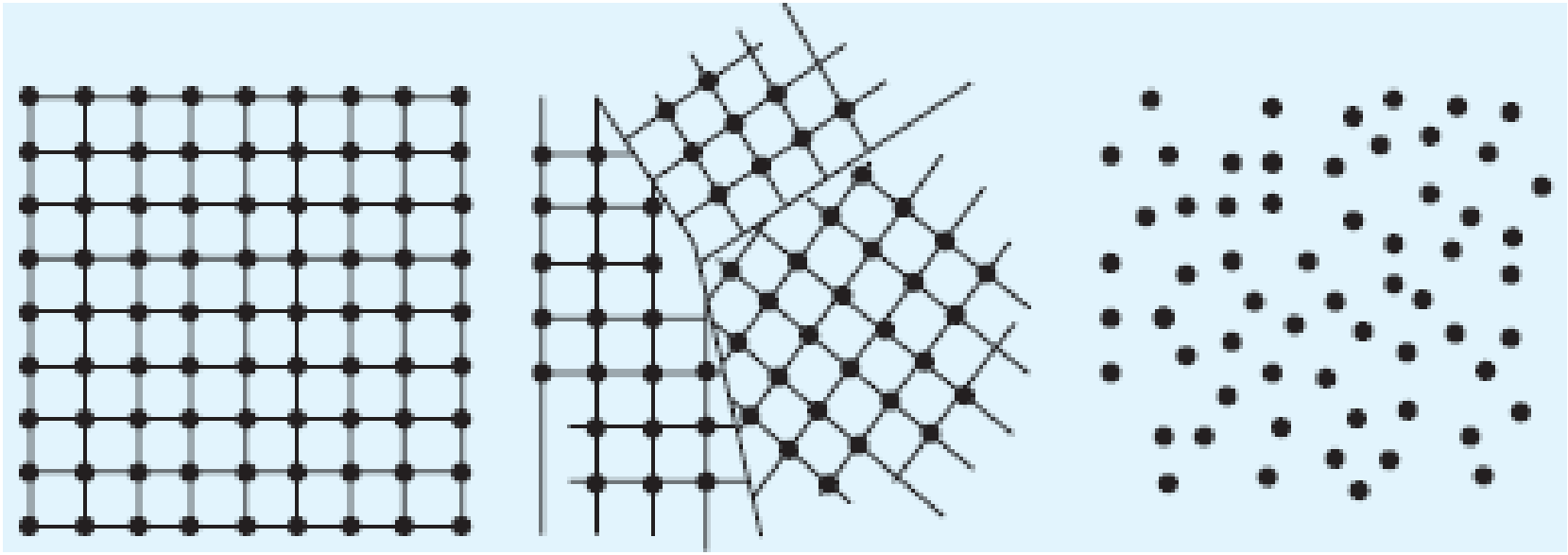
• After ion implantation, thermal annealing is required. Furnace annealing takes minutes and causes too much diffusion of dopants for some applications.

• In rapid thermal annealing (RTA), the wafer is heated to high temperature in seconds by a bank of heat lamps.

•In flash annealing (100mS) and laser annealing (<1uS), dopant ddiffusion is practically eliminated.

3.7 Thin-Film Deposition
Three Kinds of Solid

Crystalline | Polycrystalline | Amorphous



Example: Silicon wafer

Thin film of Si or metal.

Thin film of SiO_2 or Si_3N_4.

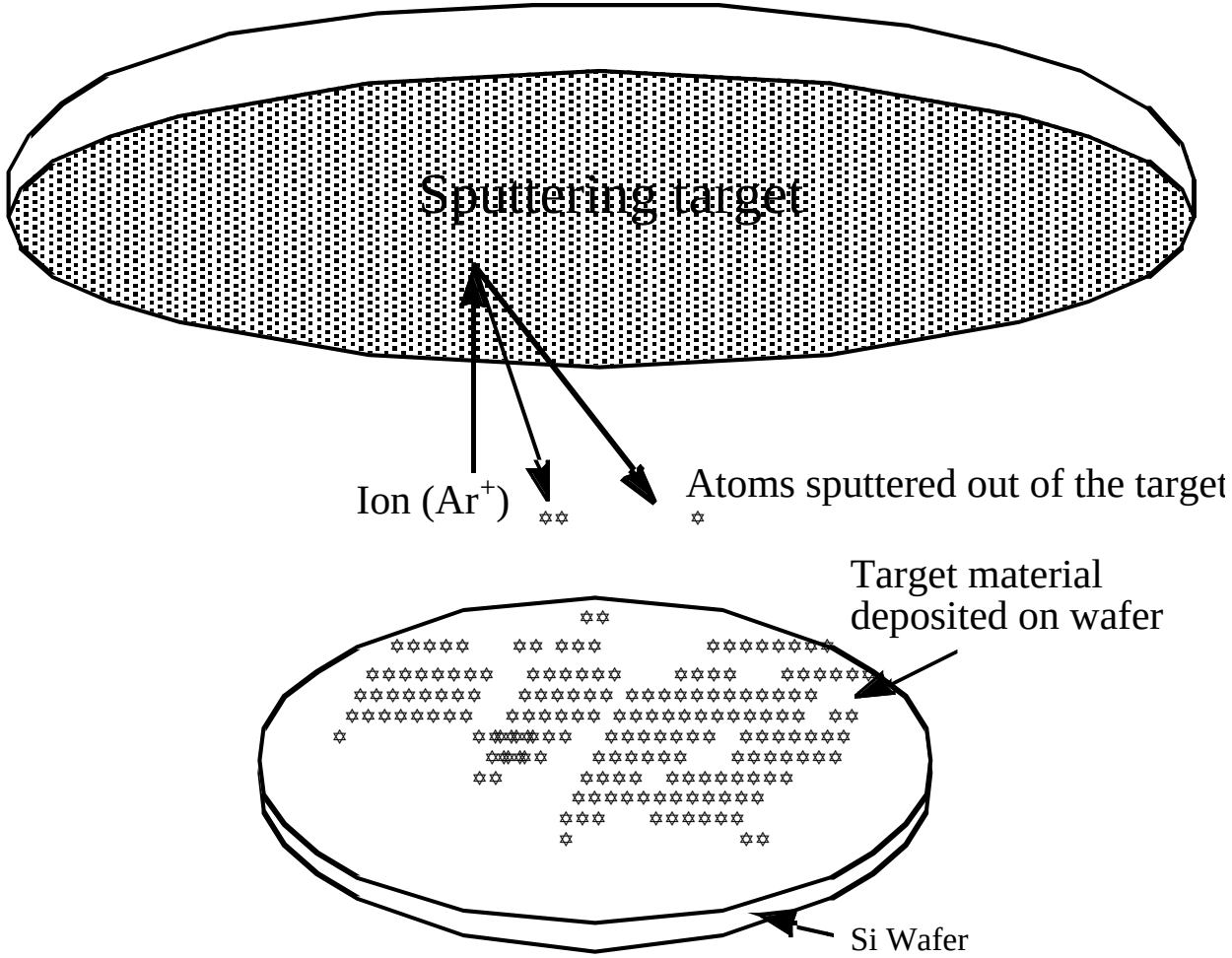
3.7 Thin-Film Deposition

Examples of thin films in integrated circuits

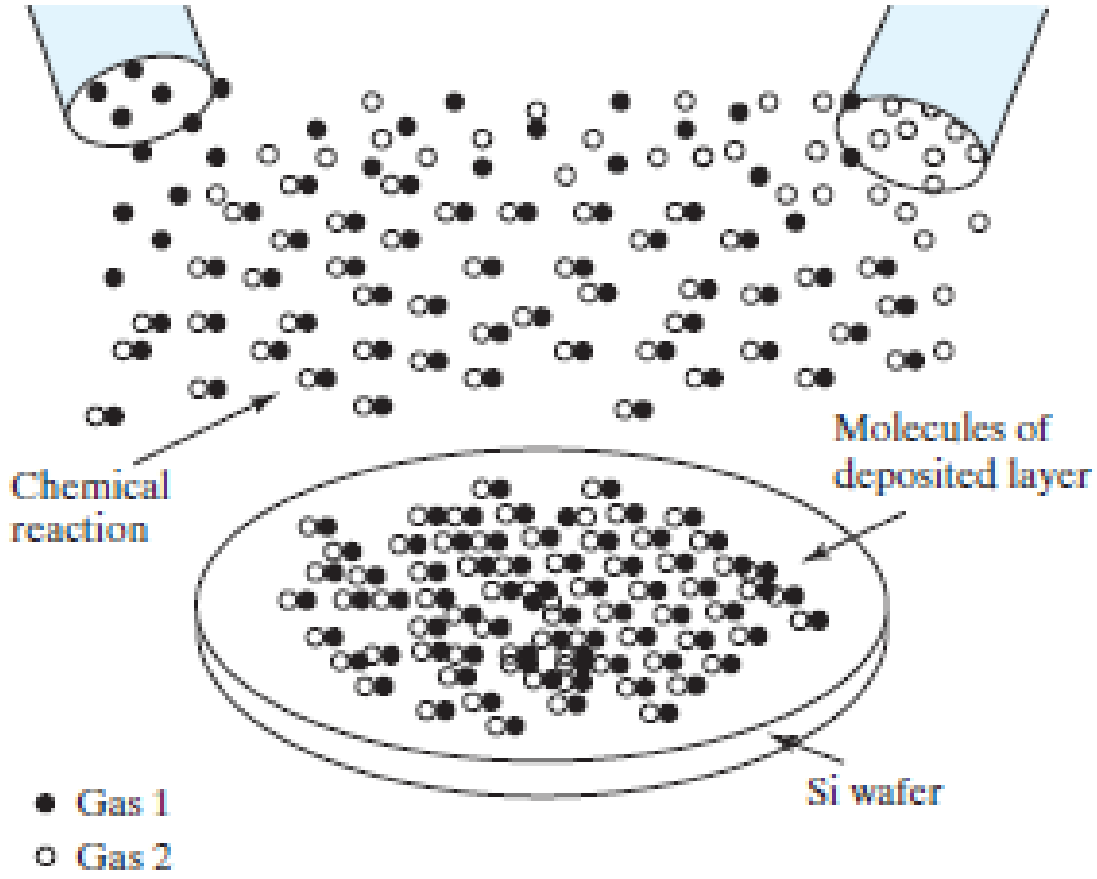
- Advanced MOSFET gate dielectric
- Poly-Si film for transistor gates
- Metal layers for interconnects
- Dielectric between metal layers
- Encapsulation of IC

3.7.1 Sputtering

Schematic Illustration of Sputtering Process



3.7.2 Chemical Vapor Deposition (CVD)



Thin film is formed from gas phase components.

Some Chemical Reactions of CVD

Poly-Si : $SiH_4\ (g) \longrightarrow Si\ (s) + 2H_2\ (g)$

Si3N4 : $3SiH_2Cl_2\ (g) + 4NH_3\ (g) \longrightarrow Si_3N_4\ (s) + 6HCl(g) + 6H_2\ (g)$

SiO2 : $SiH_4\ (g) + O_2\ (g) \longrightarrow SiO_2\ (s) + 2H_2\ (g)$

or

$SiH_2Cl_2\ (g) + 2N_2O\ (g) \longrightarrow SiO_2\ (s) + 2HCl\ (g) + 2N_2\ (g)$

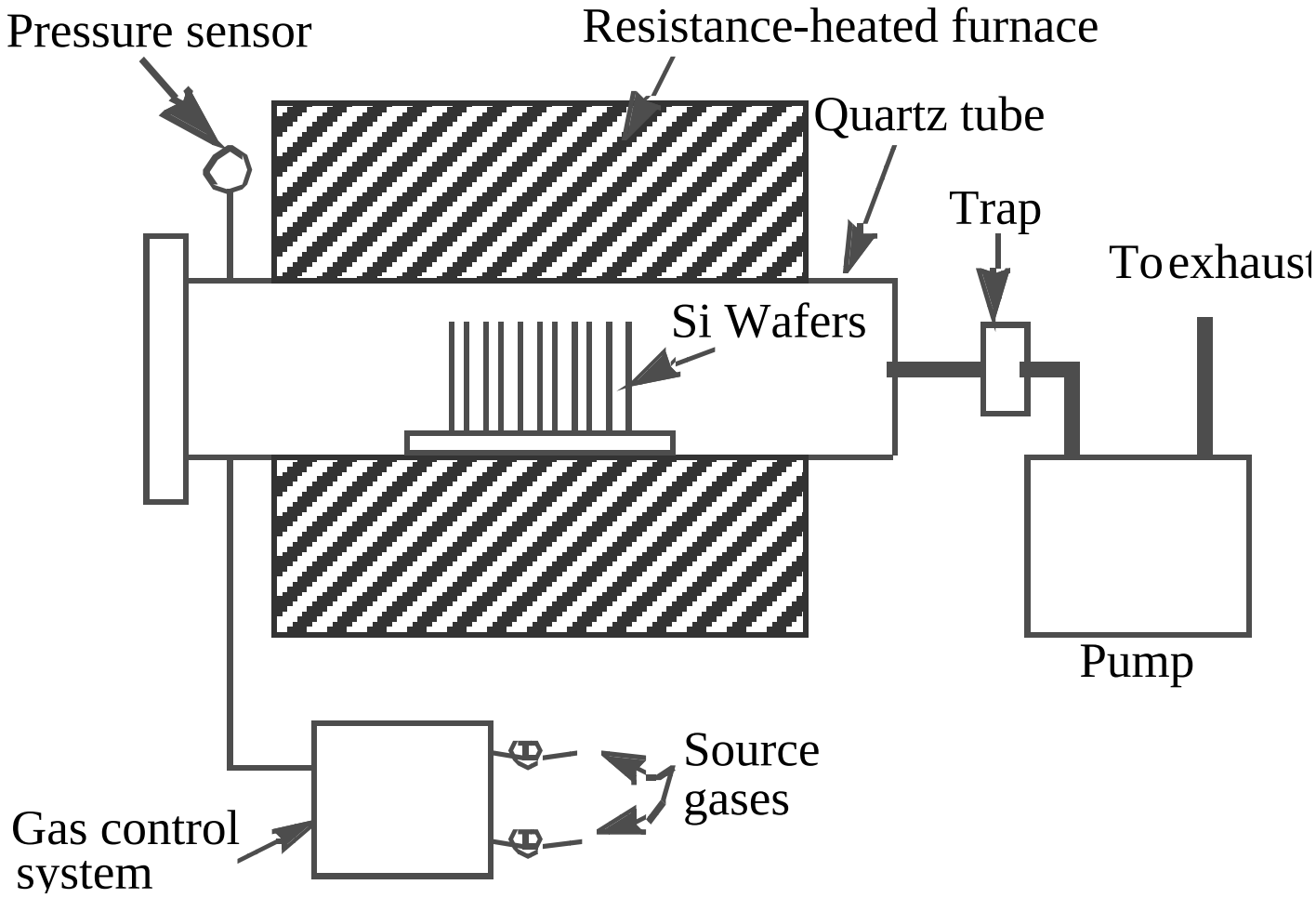
3.7.2 Chemical Vapor Deposition (CVD)

Two types of CVD equipment:

- **LPCVD (Low Pressure CVD)** : Good uniformity. Used for poly-Si, oxide, nitride.

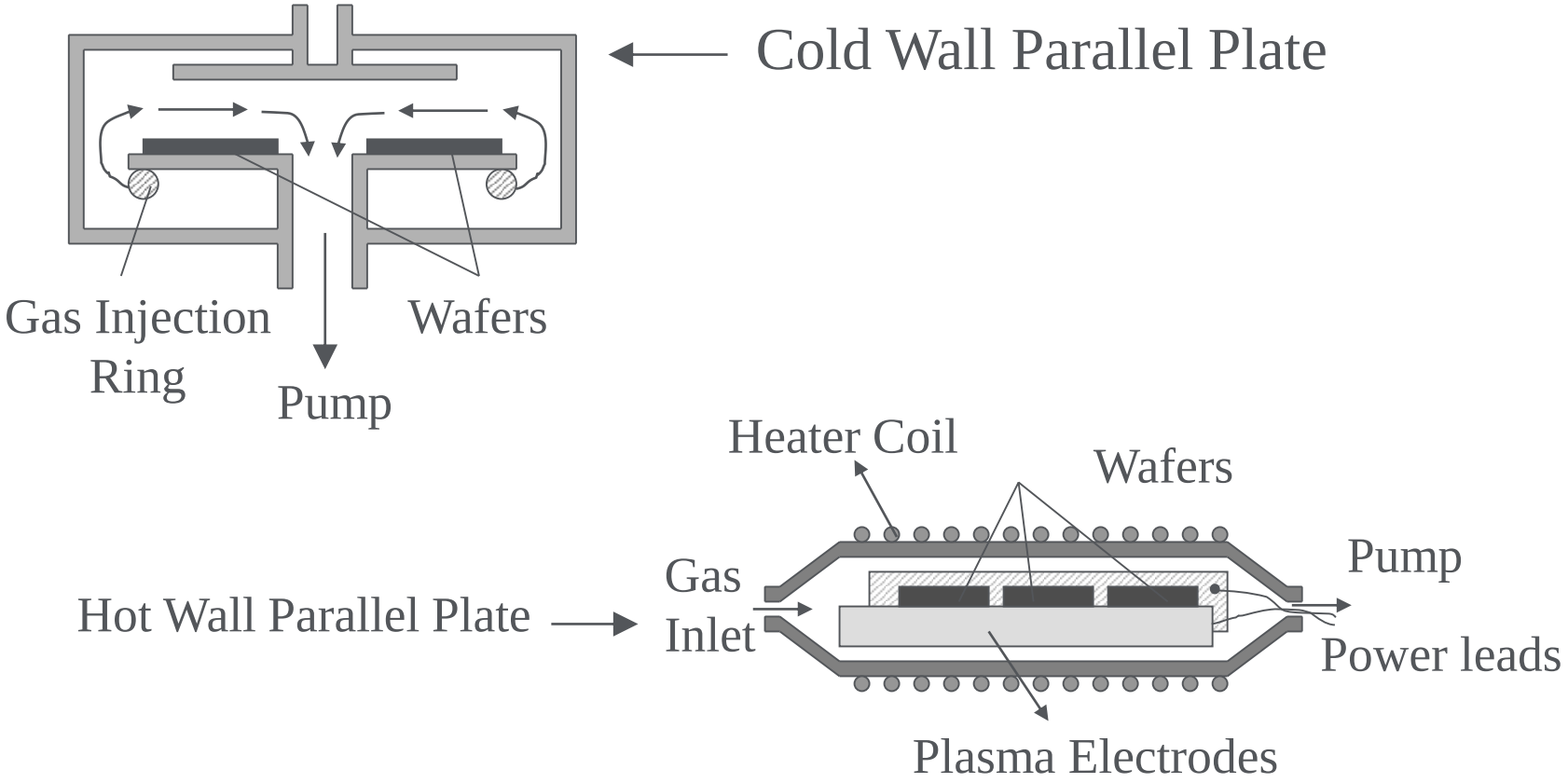
- **PECVD (Plasma Enhanced CVD)** : Low temperature process and high deposition rate. Used for oxide, nitride, etc.

3.7.2 Chemical Vapor Deposition (CVD)



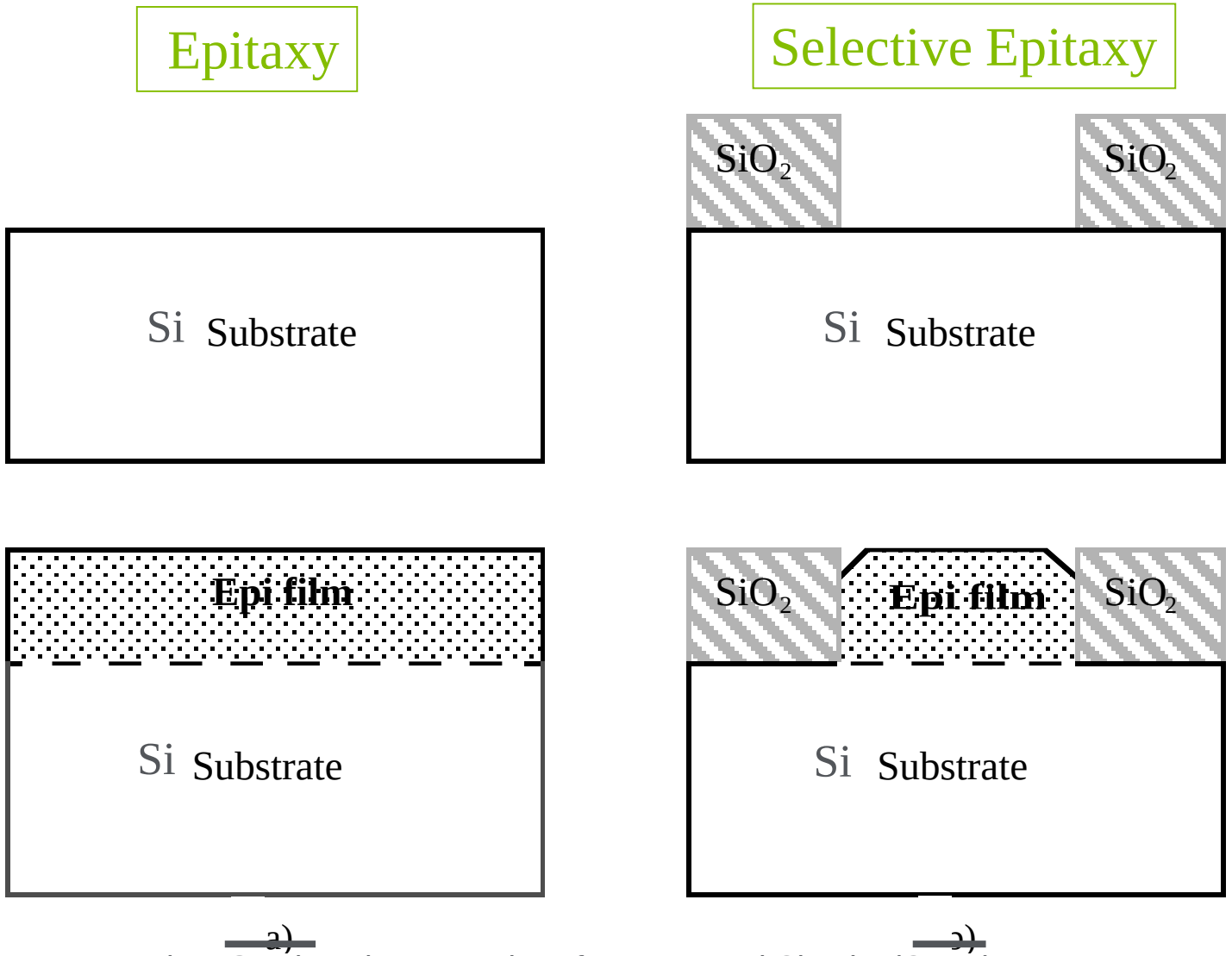
LPCVD Systems

3.7.2 Chemical Vapor Deposition (CVD)

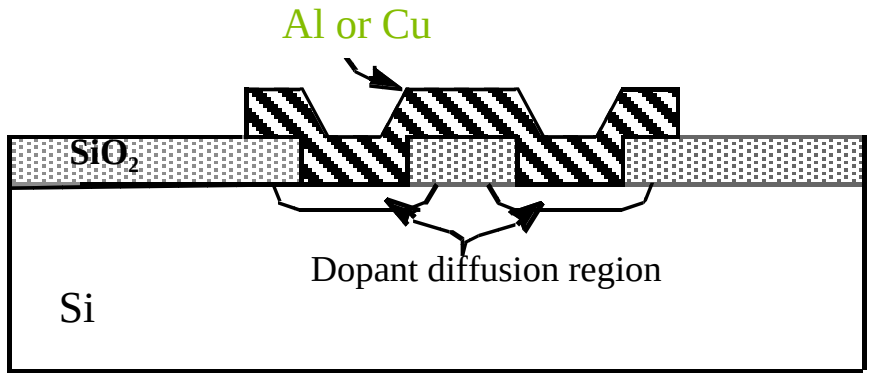


PECVD Systems

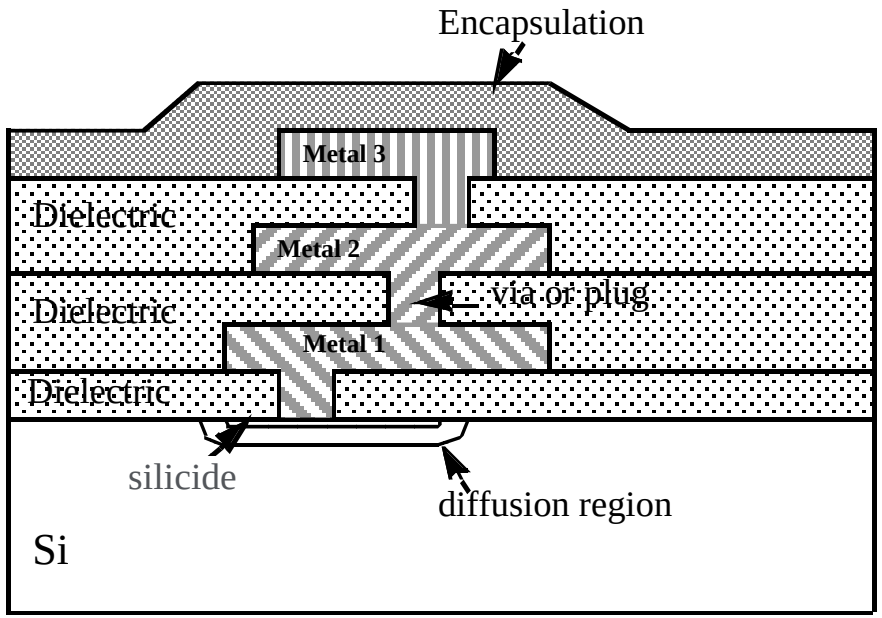
3.7.3 Epitaxy *(Deposition of Single-Crystalline Film)*



3.8 Interconnect – The Back-end Process



(a)



(b)