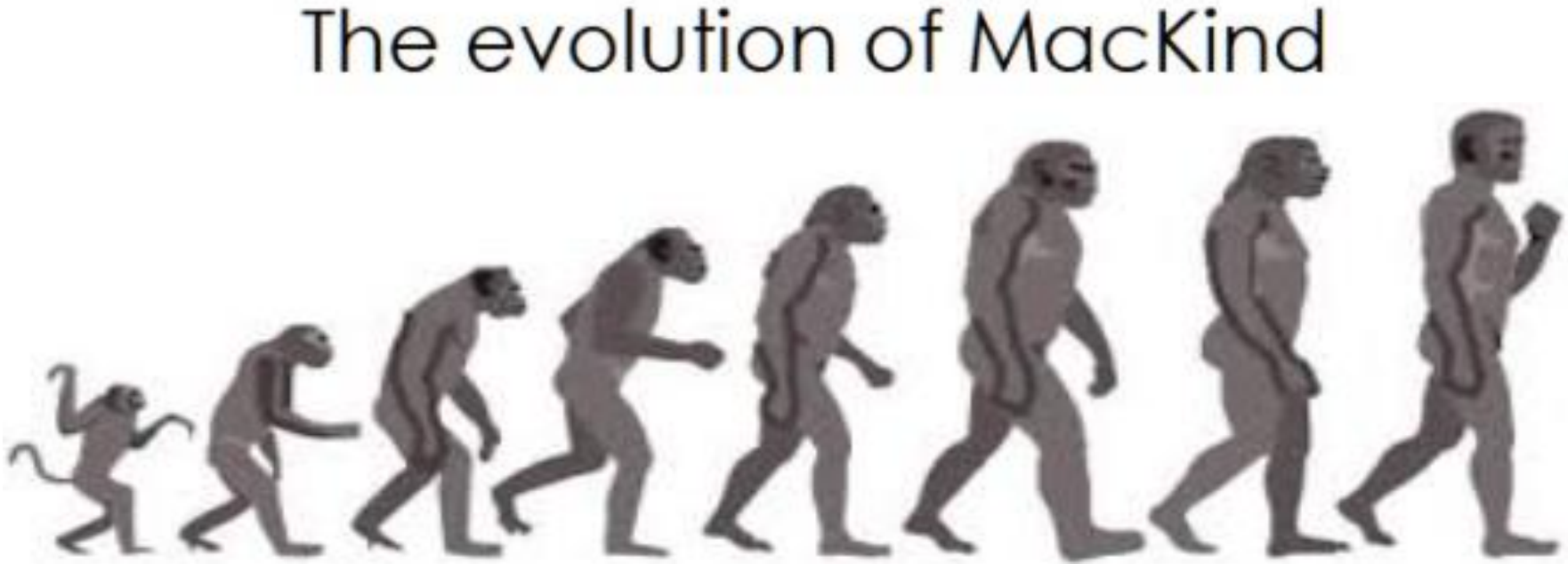
Evolving Frontiers

Evolution of Semiconductor Packaging
ATMP –Conventional vs Advanced
ATMP Market Size, Supply-Chain & Tech Trends
Manufacturing Processes

APPLIED MATERIALS®

It is all about packaging…

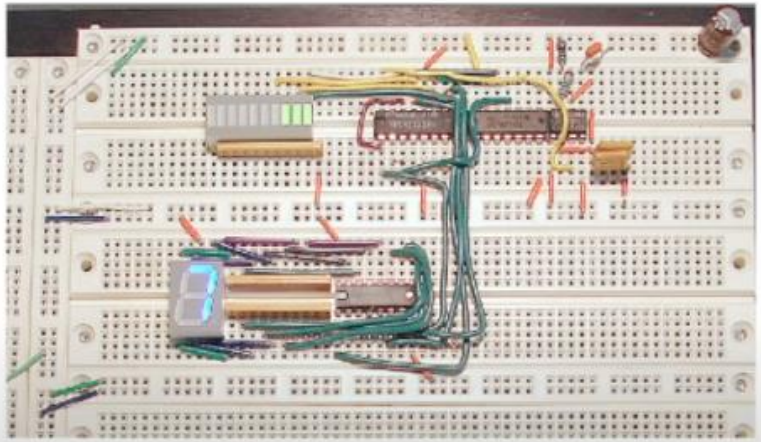


APPLIED MATERIALS®

Evolution of Semiconductor Packaging…

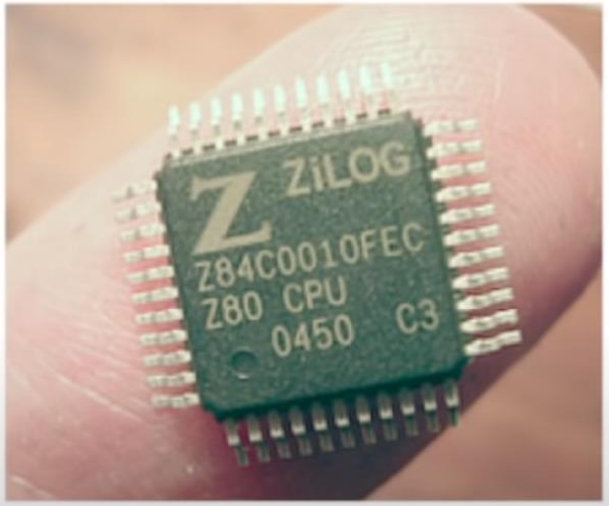
70's

Dual Inline Package (DIP)



75-80's

Quadruple Flat Package (QFP)

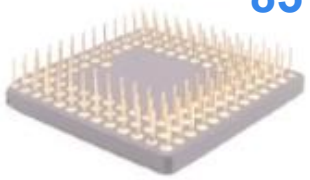


# of pins

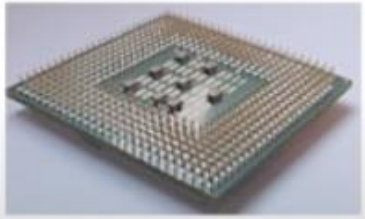
- DIP – upto 50
- QFP – upto 200

85's

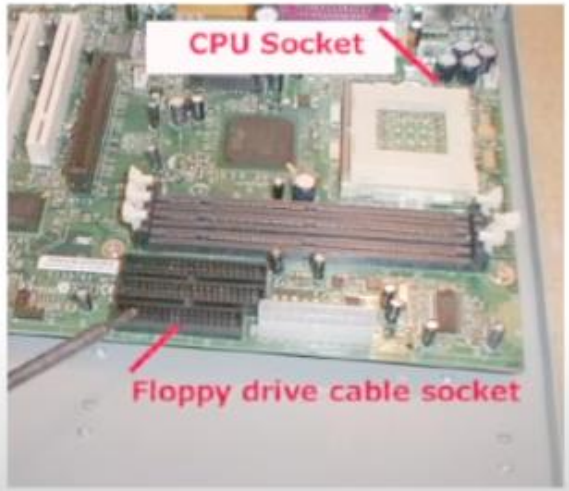
Pin Grid Array (PGA)



Motorola 68020

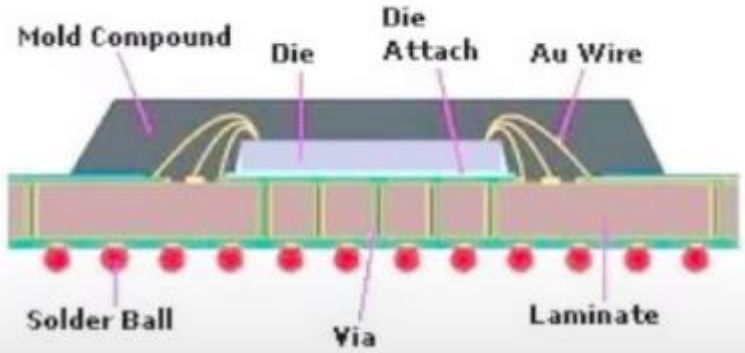


Pentium 4



90's

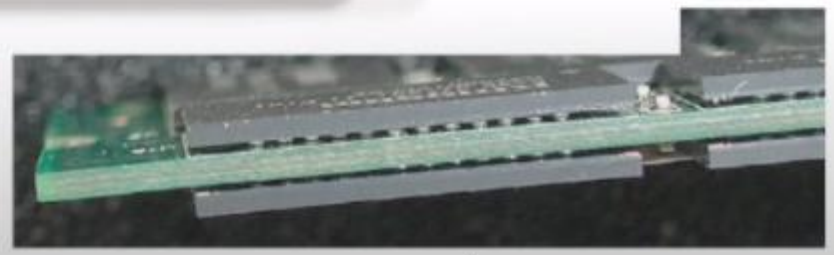
Ball Grid Array (BGA)



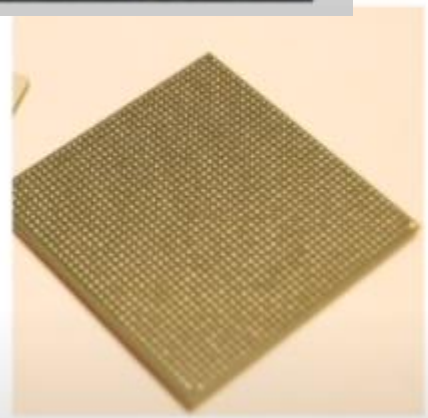
Evolution of Semiconductor Packaging…

Ball Grid Array (BGA)

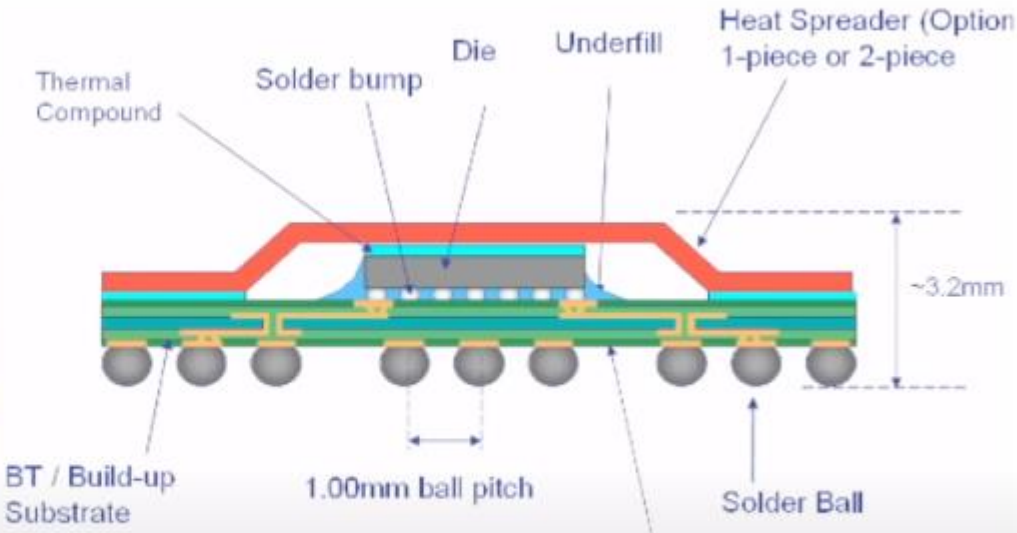
90’s



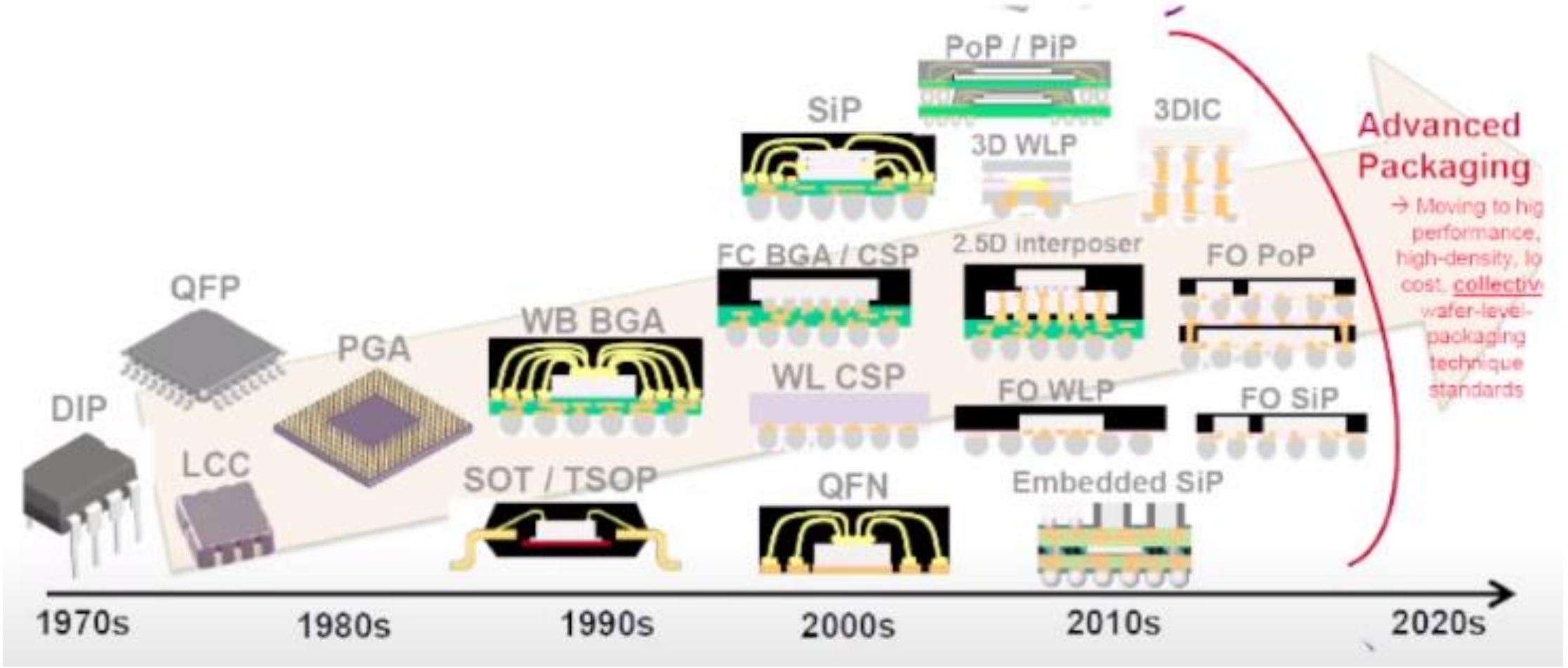
Flip Chip Ball Grid Array (FCBGA)



2000’s



Evolution of Semiconductor Packaging…



APPLIED MATERIALS

SYSTEM INTEGRATION LEVELS

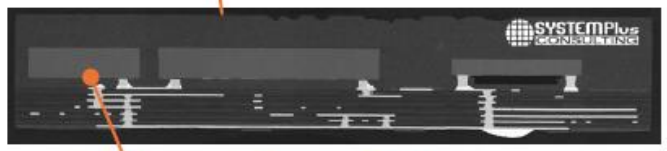
LEVEL 3:
End
Device/Equipment

iPhone 6

LEVEL 2:
Device/Equipment
Board

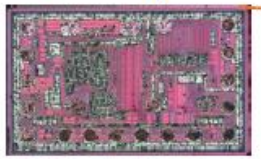
iPhone 6 PCB

LEVEL 1:
Semiconductor
Packaging

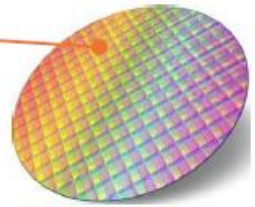


Qorvo RF SiP
in the iPhone 6s Plus

LEVEL 0:
Semiconductor
Die/Wafer

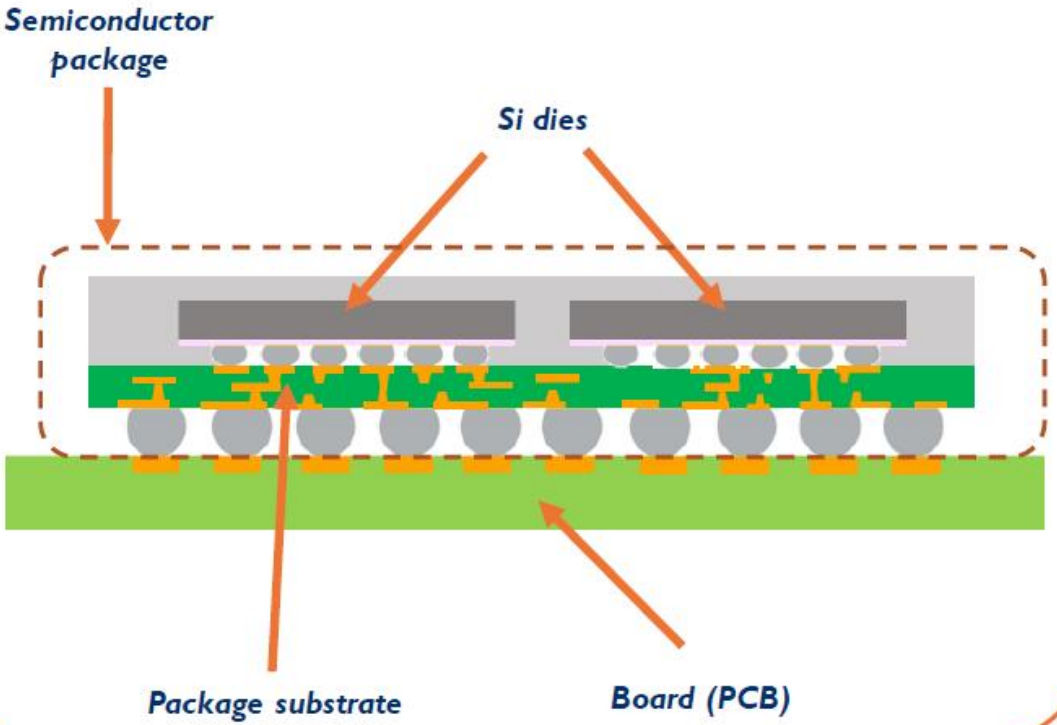


Power amplifier in
Qorvo RF SiP

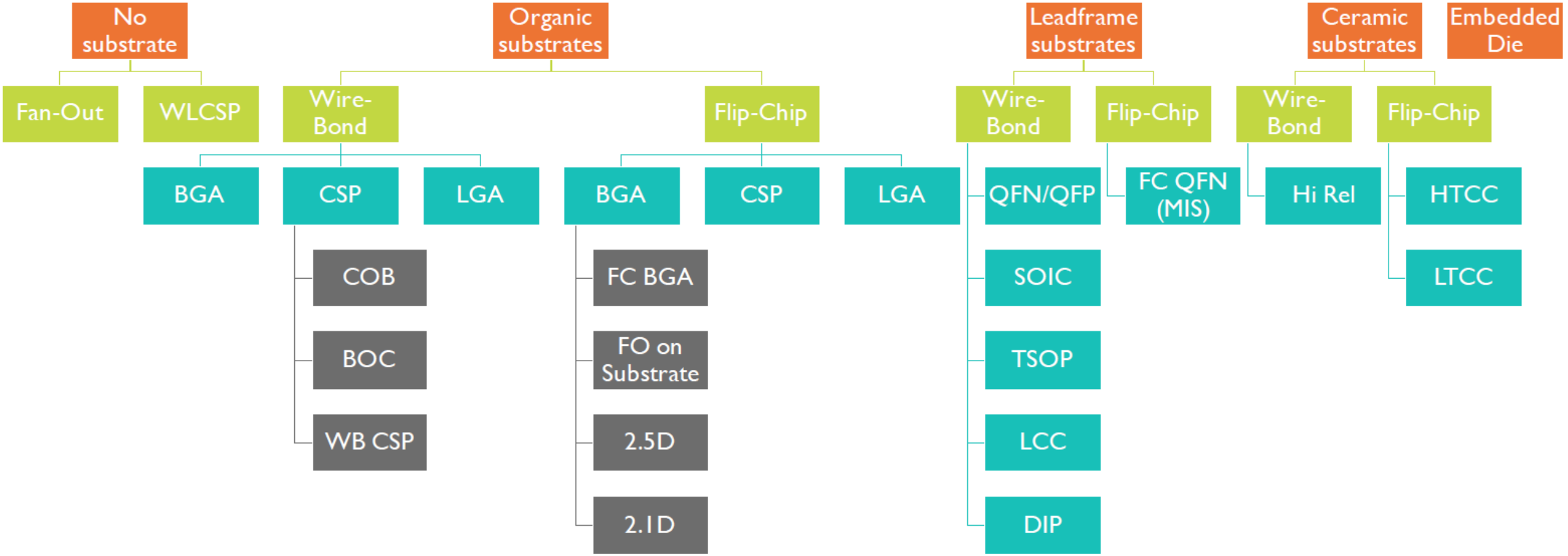


Semiconductor
wafer

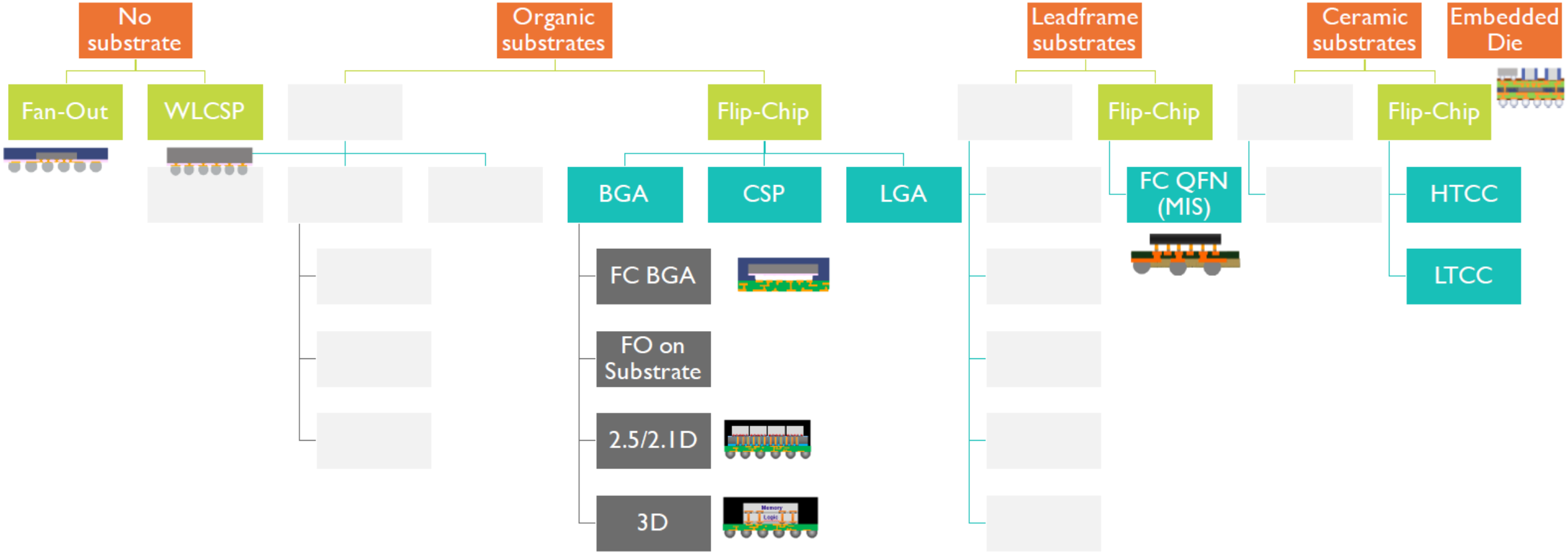
LEVEL 1+2:
Semiconductor Package + Board



PACKAGING FAMILY PLATFORMS

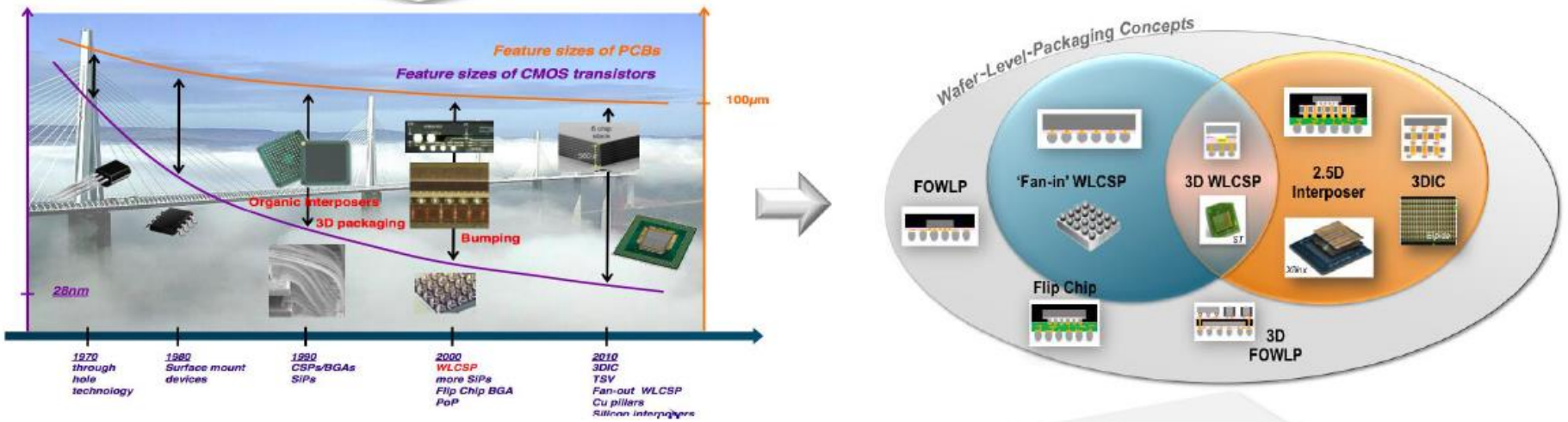


ADVANCED PACKAGING PLATFORMS



Introduction to the world of ATMP

- The evolution of semiconductor packaging technologies over the past 40 years has been driven by the need to bridge the increasing "I/O interconnect gap", between the fast decreasing silicon geometries (Moore's law) and the slower shrink of the Printed Circuit Board technologies



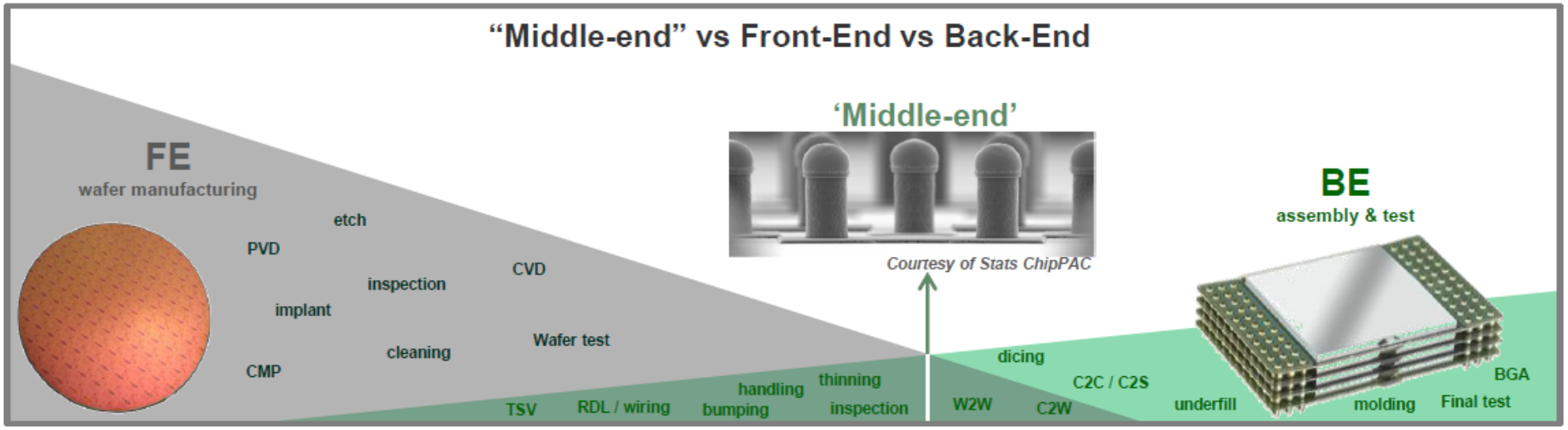
- Wafer-level-packaging market is gaining more and more significance in the semiconductor industry; it shows the greatest potential for significant future growth in the semiconductor industry.

- Historically supported by the market growth in flip-chip wafer bumping with electroplated gold, solder bumps and today copper pillars; wafer-level-packages are actually coming in many different, namely Fan-in WLCSP packages, 3D WLP, FO WLP packages, 2.5D Glass / Silicon interposers and of course 3DIC integration with TSV interconnects.

WLP – the 'Middle-end" process

- **Wafer level packages are true "Middle-end' technologies, leverage similar type of process manufacturing know-how**

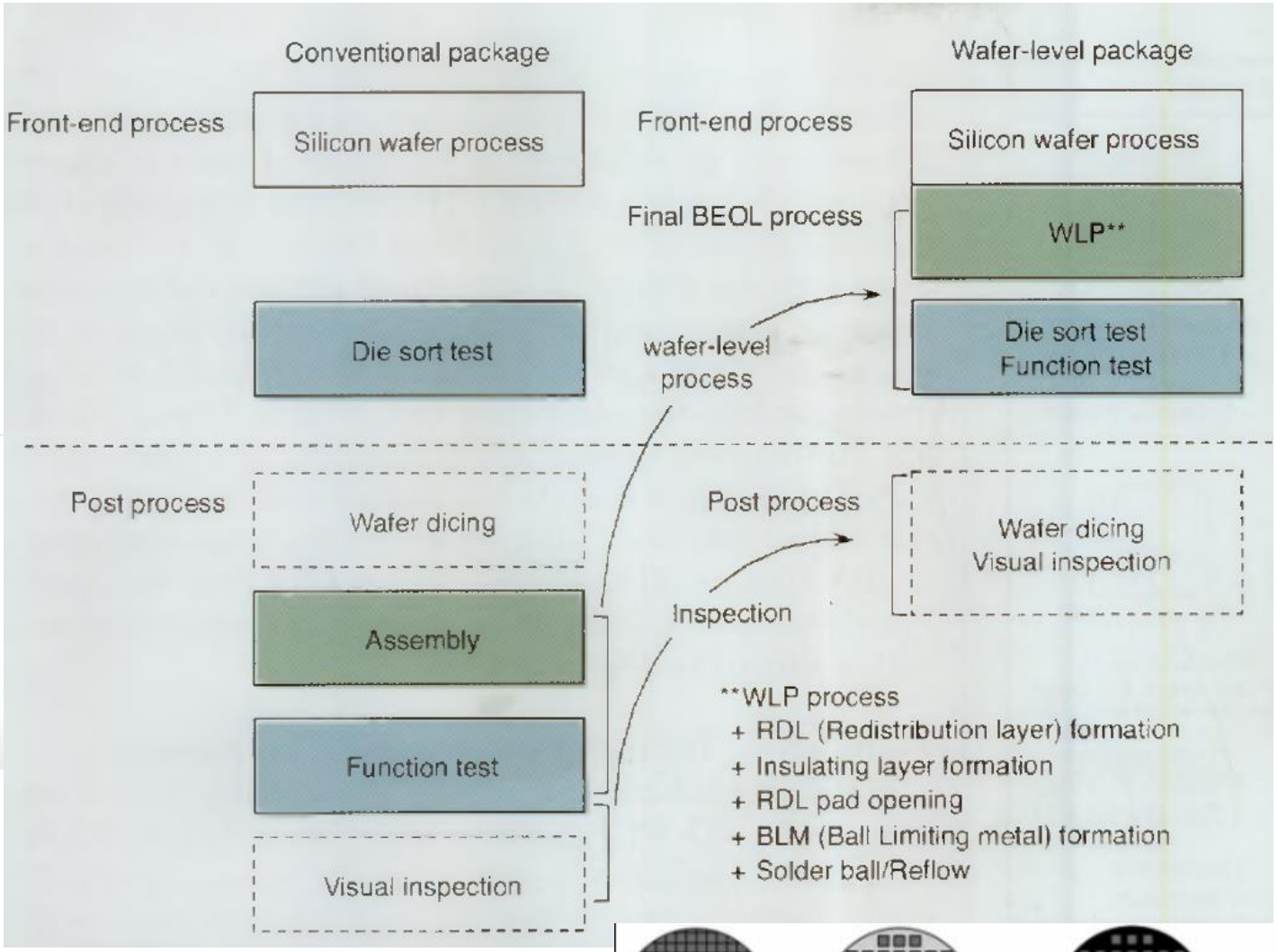
⇒ **Middle end technologies are found in the overlap area between the IDMs or CMOS foundries' back-end of line (BEOL) wafer fabs and the the back-end wafer bumping assembly facilities of the OSATs and wafer bumping houses**



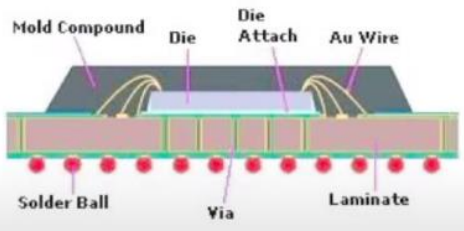
- **Middle-end is a strategic area where Foundries, OSATs, WLP Houses and IDMs stepped in, an infrastructure that has emerged by itself in the last 5 years.**
- **Middle-end infrastructure is growing and is the leading driver and the fastest growing semiconductor packaging technology with more than 18% CAGR in units over the next 6 years**

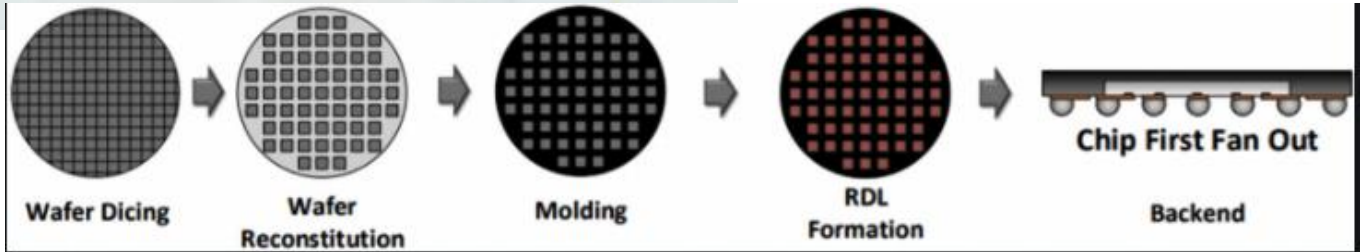
APPLIED MATERIALS

Packaging Process Comparison: WLP vs Conventional



Ball Grid Array (BGA)

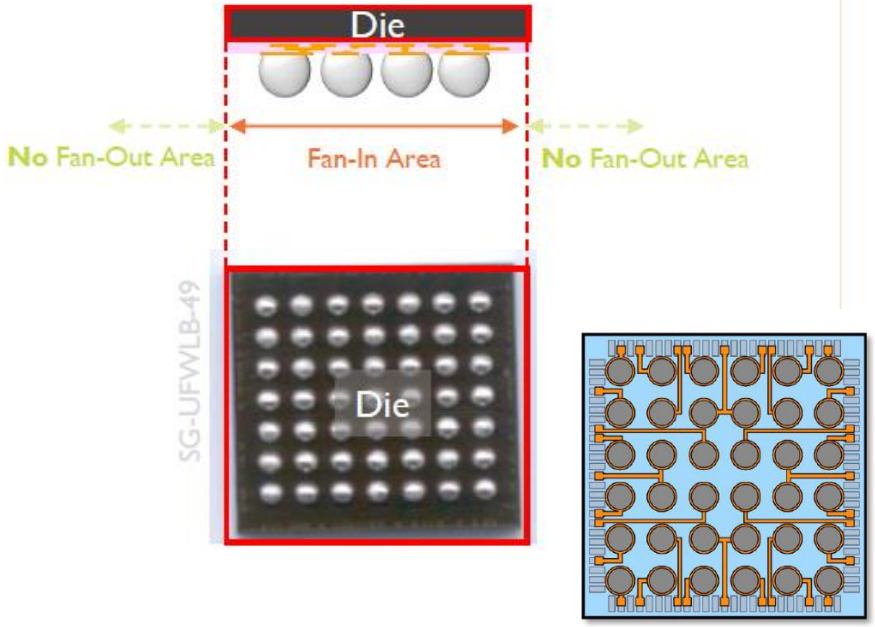




FI-WLP vs FO-WLP

Package size and connections array are flexible and independent from die size.

Fan-In WLP
restricted to chip size



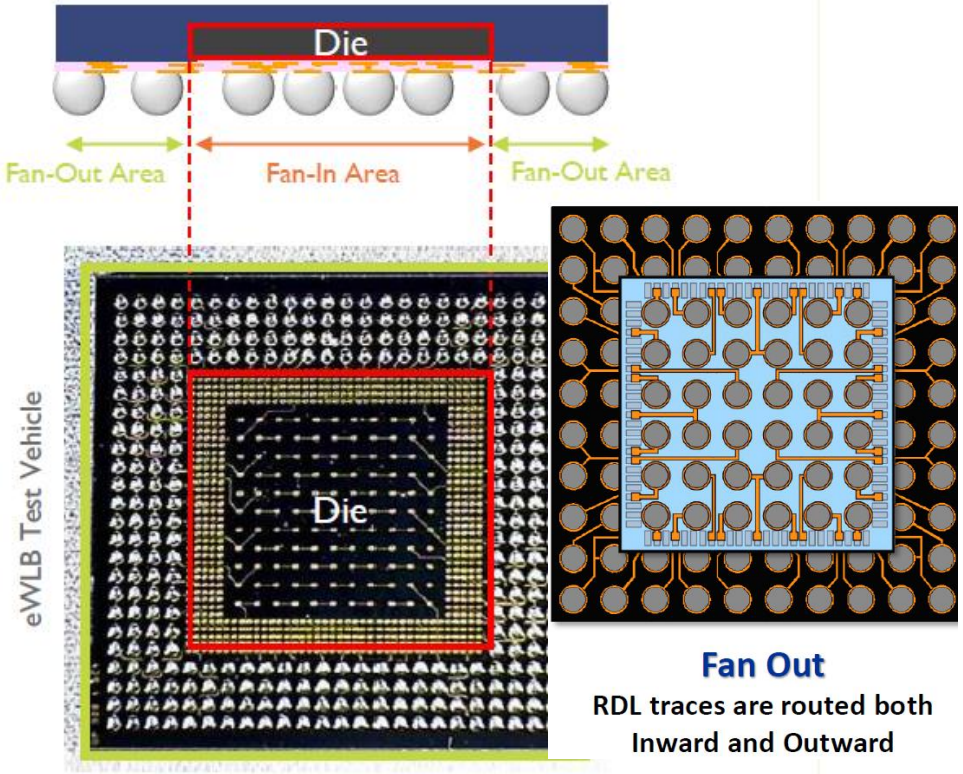
Fan In

All RDL traces are routed inward

Fan-In WLPs are chip-size packages:

- All balls must fit under the chip surface
- Interconnects pitch must be adapted to the chip size

Fan-Out package
offers fan-out possibility



Fan Out

RDL traces are routed both Inward and Outward

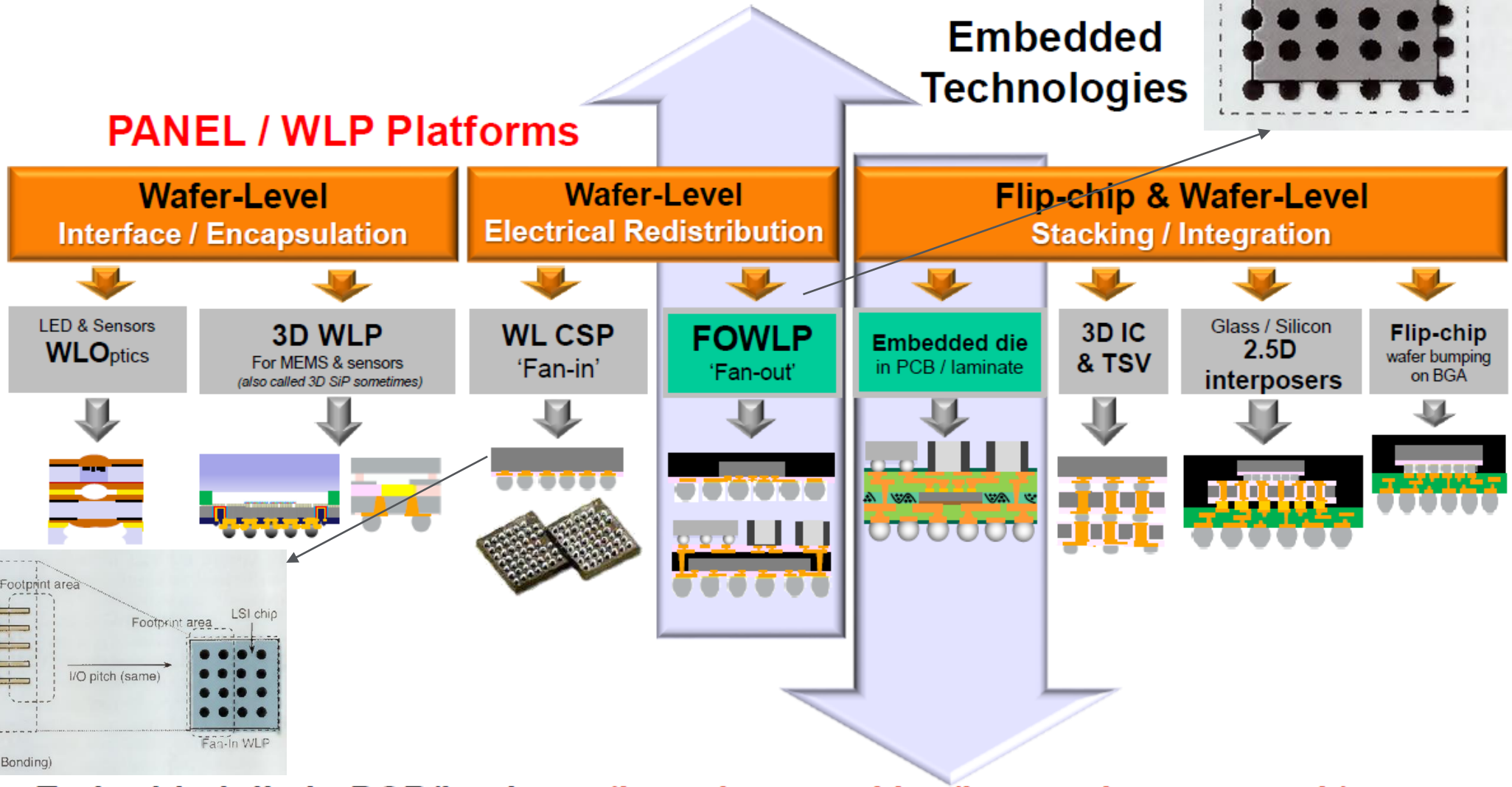
Package design of Fan-Out package is independent of chip size:

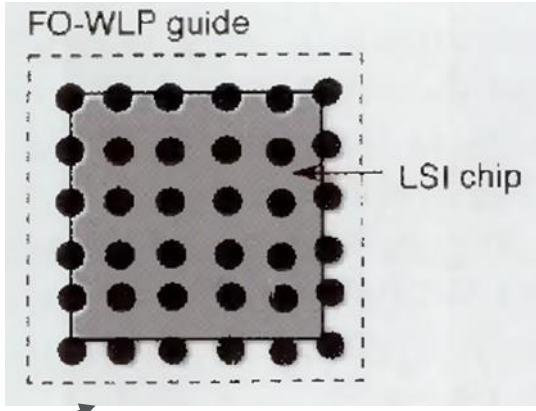
- Fan-Out Package covers both Fan-In and Fan-Out areas
- Fan-Out area adaptable to needs
- No restrictions for ball pitch

External Use

Embedded Wafer Level Packaging

- **FOWLP** (based on electrical redistribution)





- **Embedded die in PCB/laminate** (based on stacking/integration approach)

APPLIED MATERIALS