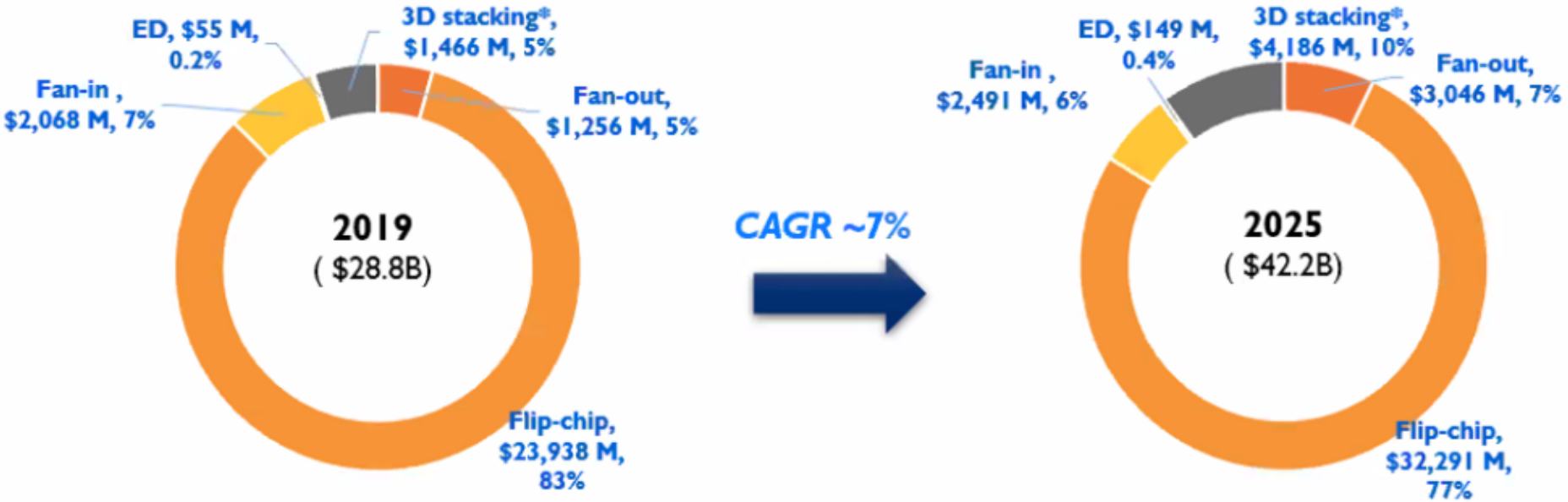
ADVANCED PACKAGING REVENUE FORECAST 2019-2025

Advanced Packaging REVENUE SPLIT by packaging platform

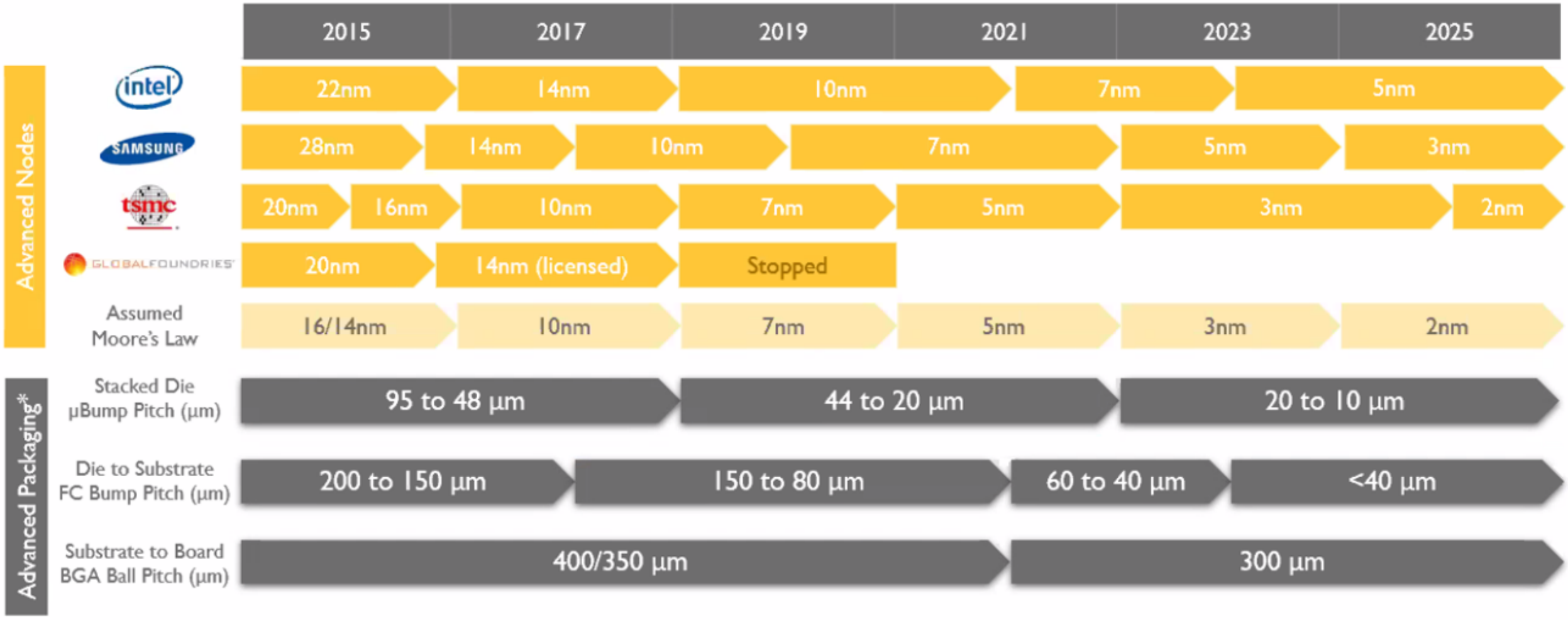


Flip-chip	$CAGR_{2018\text{-}2025}$ ~ 5.9%%
Fan-out	$CAGR_{2018\text{-}2025}$ ~ 16%
Fan-in WLP	$CAGR_{2018\text{-}2025}$~ 3.2%
3D Stacking	$CAGR_{2018\text{-}2025}$ ~ 21.3%
Embedded Die	$CAGR_{2018\text{-}2025}$ ~ 18%

- *The Advanced Packaging market was worth ~$28.8B in 2019. It is expected to grow at ~ 7% $CAGR_{2019\text{-}2025}$ to reach ~$42.2B in 2025.*
- *Highest revenue CAGR expected from 2.5D / 3D stacking IC, ED (in laminate substrate) and Fan-Out, 21%, 18% and 16%, respectively, as high volume products further penetrate the market: FO in mobile, networking, automotive; 2.5D/3D TSV in AI/ML, HPC, datacenters, CIS, MEMS/sensors; ED in automotive and medical.*

- *NOTE:*
  - *Values represent packaging services (assembly and test) and do not include FEOL Si die processing*
  - *TSV* includes portion of package revenue not included in Flip-chip or fan-in*

TECHNOLOGY ROADMAP: FROM NANO-SCALE TO MICRO-SCALE..



Industry is looking into the growing importance of functional roadmap

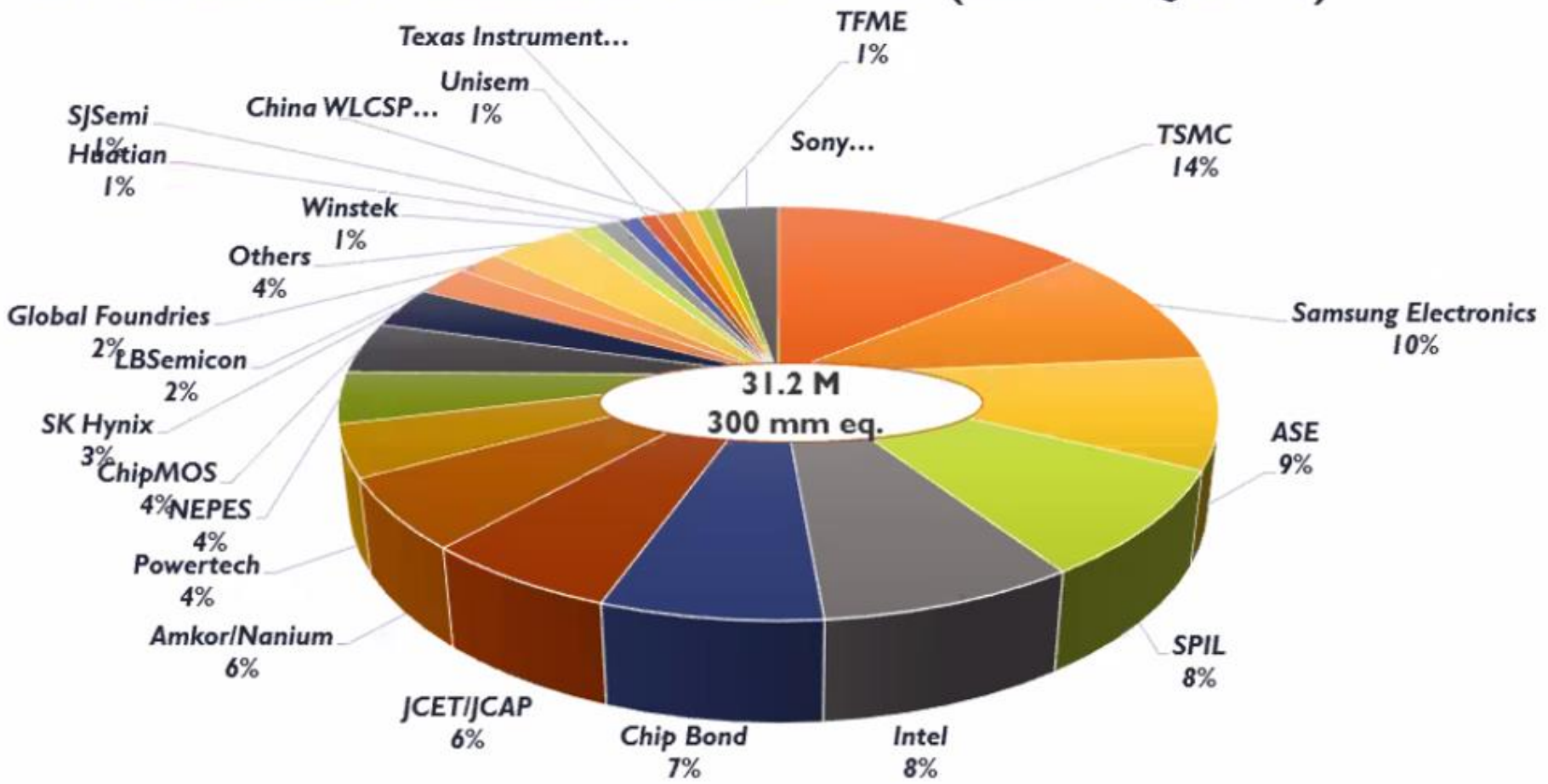
Advanced Packaging is essential to bridge the scale-gap between die and PCB

Average trends based on technology and industry expectation
*Minimum dimension

ADVANCED PACKAGING 2019 WAFER SPLIT BY MANUFACTURER

TEN players, which includes 2 IDMs (Intel, Samsung), a foundry (TSMC), the top 5 global OSATs (ASE, SPIL, Amkor, PTI, JCET) together with Nepes and Chipbond, process approximately 75% of Advanced Packaging wafers.

2019 ADVANCED PACKAGING WAFER SPLIT (300MM EQ WSPY)



NOTE:

- This pie chart represents superpositions of all Advanced Packaging platforms (Fan-in/Fan-out WLP, Flip-chip including 2.5D/3D and embedded die.
- Flip-chip values are entered as total capacity, fan-in, fan-out, 3D stacking and embedded die as total production.
- Flip-chip production values were not available by customer – global utilization is at ~85-90% of capacity.

FINANCIAL OVERVIEW FOR TOP 25 OSATS

Revenue in 2019

Large OSATs were separated from the rest.

Top 8 OSATs continued with heavy investment in CapEx and R&D.

TOP 25 OSAT ranking by 2019 revenue [$M]

TSMC ranks between 3rd &4th

If counted separately, SPIL revenue in 2019 is $2.88B, which will place it as 4th among global OSATs.

Players not within the Top 8 rankings need to catch up. Otherwise, they risk being acquired or incurring losses in business.

Top OSATs with heavy investments were creating a disparity with the rest of the pack.

Top 8 OSATs now include 3 manufacturer HQ-ed in China. UTAC maintained its 8th spot.

Companies in the tail are at a higher risk if there is no differentiated technology or IP for merger and acquisition as an exit strategy.

Développement

**Note: SPIL included in ASE figures from 2019 onwards

SEMICONDUCTOR SUPPLY CHAIN - 2020

Semiconductor production chain

PCB and substrate component suppliers

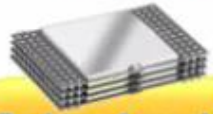
Equipment/materials suppliers

Passive components, connectors etc.

Substrate material suppliers
(FR4, BT resin, Cu clad, etc.…)

Package substrate laminate suppliers

PCB suppliers



Design
of chip & package

Silicon
Manufacturing
« Front-end »

Wafer Level Packaging
« Middle -end »

Package Assembly & Final Test
« Back-end »

Sub-Module / Sub-systems
Design & Assembly

System / Product

IDMs (Integrated Device Manufacturers)

Fab-light players (outsourcing + focused investment in manufacturing & critical IP)

Integrated wafer / package manufacturing foundries

WLP houses (no need for traditional substrate)

OSATs

OSATs with module/**EMS** capability

PCB houses with Embedded die capability

OEMs (Original Equipment Makers)

ODM / EMS / DMS

Fab-less IC players

Wafer foundries

Wafer Bumping houses

Front-end related materials suppliers

FE related equipment suppliers

BE Packaging materials suppliers

BE Packaging equipment suppliers

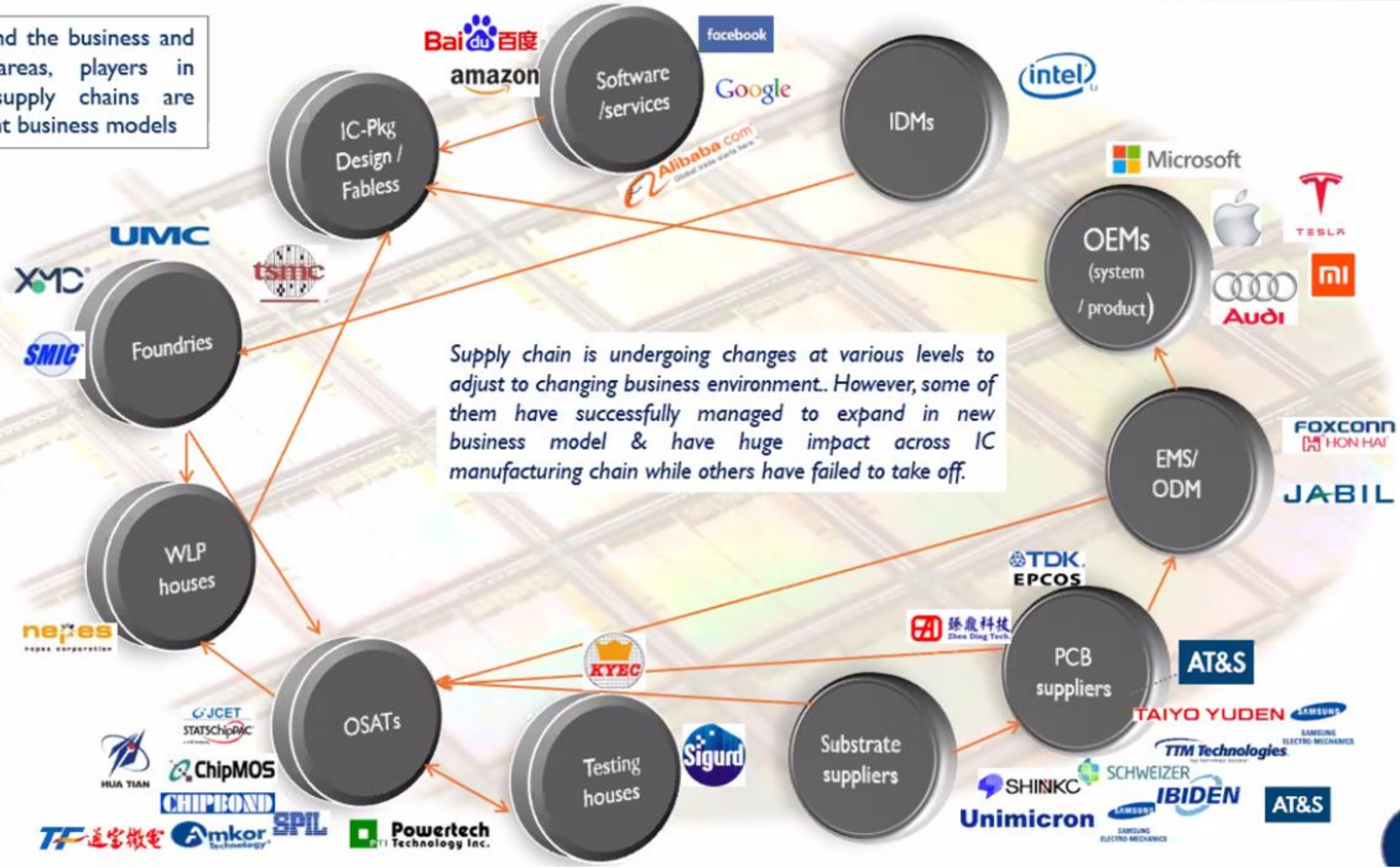
SMT material suppliers

SMT equipment suppliers

Passive components, connectors, etc.

MOBILITY ACROSS SEMICONDUCTOR SUPPLY CHAIN AT VARIOUS LEVELS

In order to expand the business and explore new areas, players in semiconductor supply chains are moving to different business models

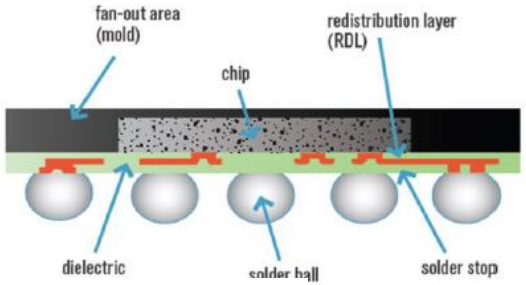


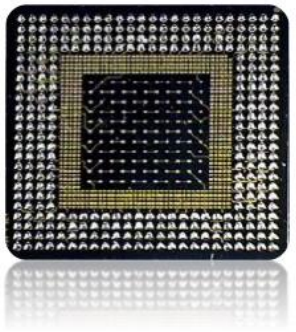
OSATS PACKAGING BUSINESS CANNIBALIZATION TREND

- *Packaging / assembly business was traditionally domain of OSATs & IDMs.*
- *Players from different business models viz. Foundries, substrate/PCB suppliers, EMS/DM are entering the assembly /packaging business & cannibalizing the OSAT business.*

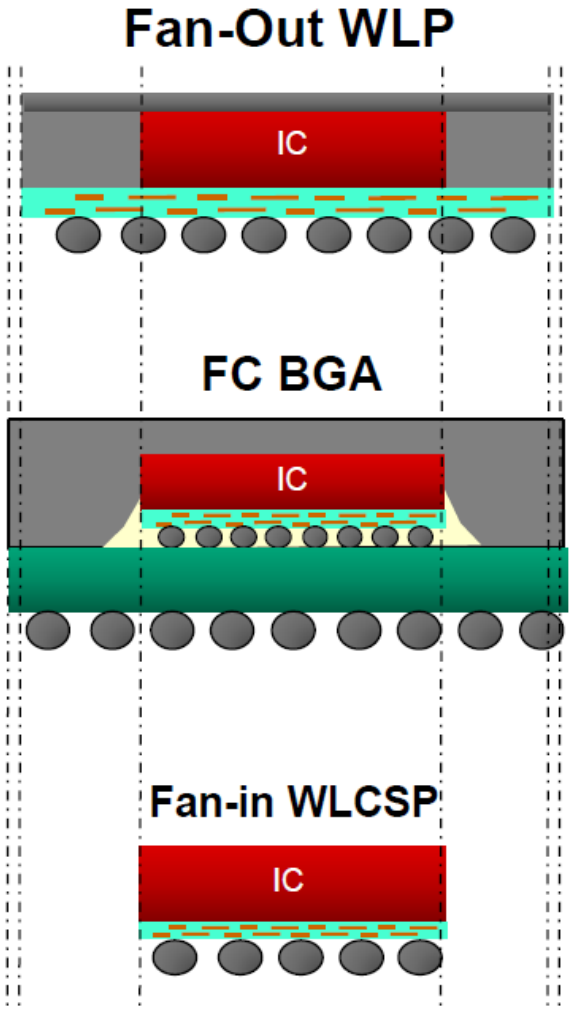
Total IC packaging business: $67B (2019)

Fan-Out Wafer Level Package

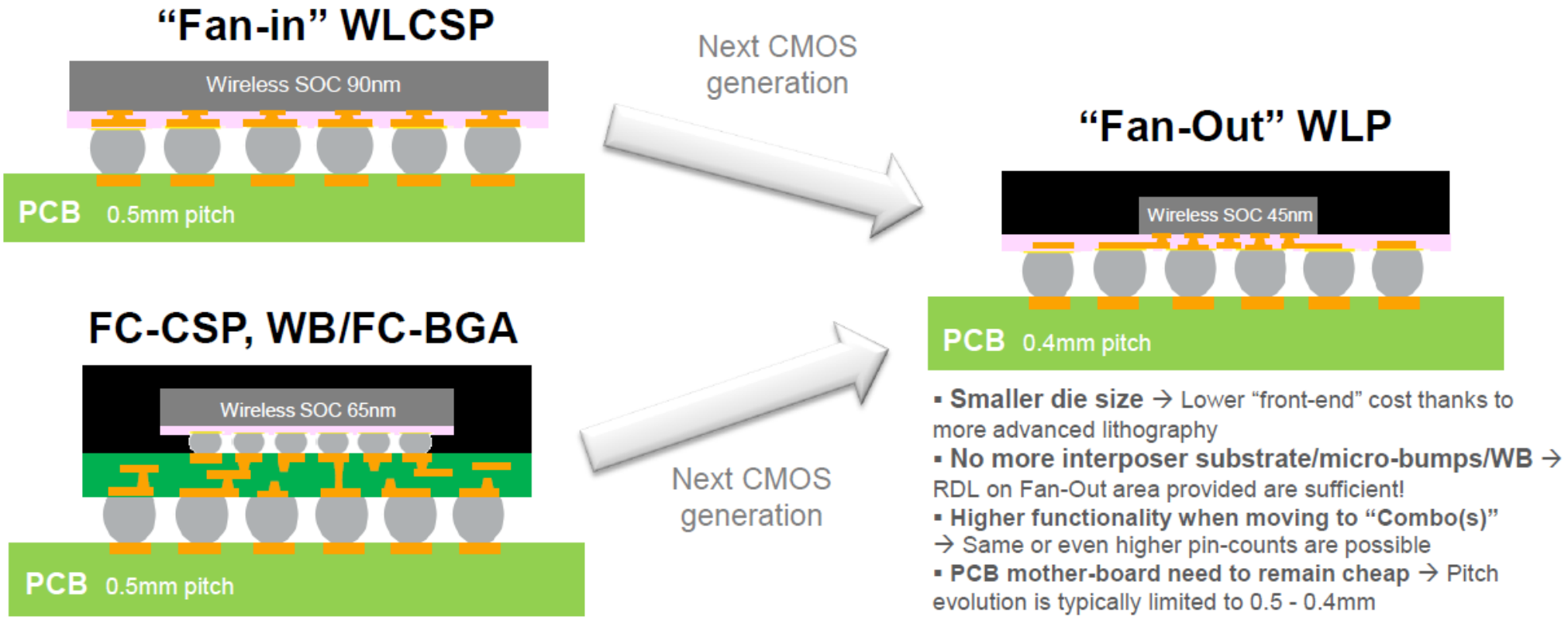




- **Fan-out Wafer Level Packages like eWLB offer the following differentiated advantages**
  - **Over flip-chip BGA:**
    - Slightly smaller footprint (clearance distances to the edges are smaller)
    - Thinner package
    - Substrate-less package (shorter interconnections meaning higher electrical performance and cheaper in the long run)
    - Future potential for SiP and 3D integration
    - Lower thermal resistance
    - Simplified supply chain infrastructure
  - **Over fan-in WLCSP:**
    - Higher board-level reliability
    - Fan-out area to counter the pad limitation issue, adaptable to customer needs
    - Only confirmed good dice are packaged
    - Potential for SiP integration
    - Lower thermal resistance
    - Built-in back-side protection
    - No restriction in bump pitch



FO WLP – Cost Motivation to continue Die Shrinkage



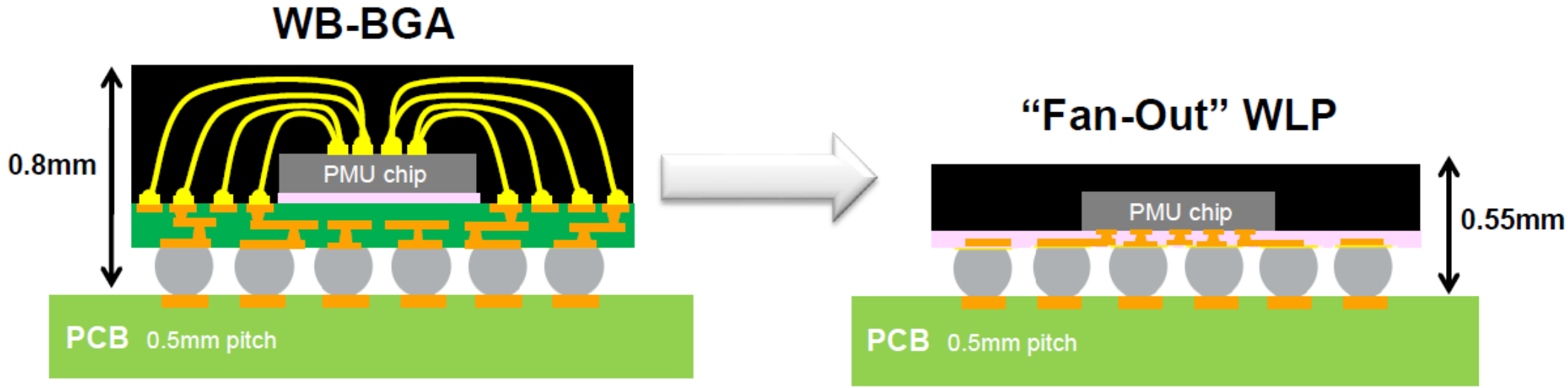
- **Smaller die size** → Lower "front-end" cost thanks to more advanced lithography
- **No more interposer substrate/micro-bumps/WB** → RDL on Fan-Out area provided are sufficient!
- **Higher functionality when moving to "Combo(s)"** → Same or even higher pin-counts are possible
- **PCB mother-board need to remain cheap** → Pitch evolution is typically limited to 0.5 - 0.4mm

- **Filling the I/O gap between IC and PCB evolution**
  - **Some restrictions are appearing at the package level, since global chip trends tend toward smaller chip areas with an increasing number of interconnects: so the shrinkage of the pitches and pads at the chip/package interface is happening much faster than the shrinkage at the package/board. As a result:**
    - FC-CSP, WB/FC-BGA package cost is increasing fast with I/O density (mainly due to interposer substrate cost)
    - Fan-in WLCSP are substrate-less but face inherent limitations due to available die area for re-routing

→ Fan-out WLP has the potential to realize any number of interconnects with standard pitches at any shrink stage of the wafer node technology

APPLIED MATERIALS

FO WLP – “Thickness” Motivation



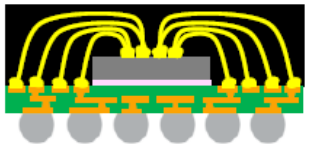
- **I/O pads are all located at the center of the die** → Front-end IC design constraint!
- **Issues are**: package height (necessary for Wire-Bonds) and thermal dissipation (flip-chip packages would be better)

- **No Wire-Bond** → Lower package height
- **Better heat dissipation** → FC configuration
- **No more interposer substrate/micro-bumps/WB** → RDL on Fan-Out area provided are sufficient!

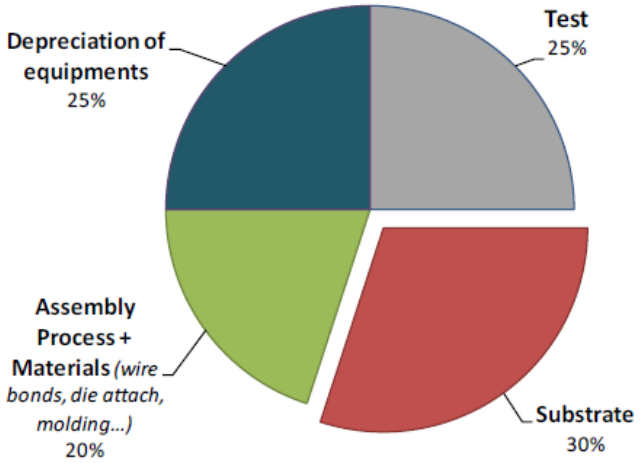
- **Meeting with new form factor and package performance**
  - **Some specific Power Management Units (PMU) have > 120 I/Os pads, all located at the center of the PMU chip due to specific IC design reasons. Using Wire Bonds takes a lot of height to connect the chip to the UFBGA substrate → Move to FC-BGA/FOWLP**
  - **First simulations show that electrical performance and heat dissipation are expected to be better than WB-BGA/FC-BGA configurations (please see next slides)**

APPLIED MATERIALS

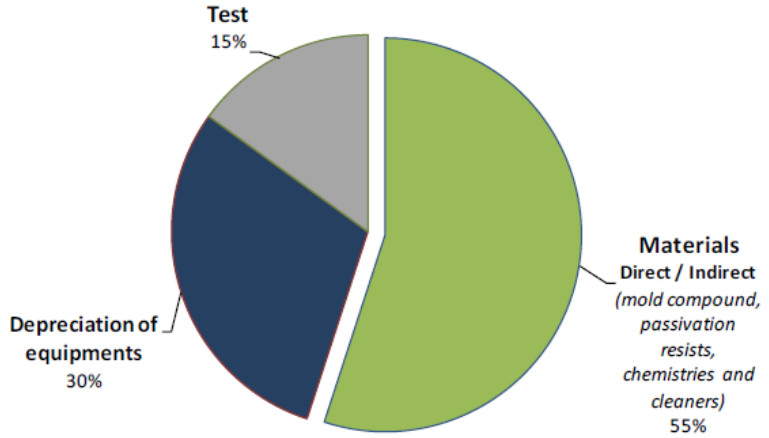
BGA vs FOWLP Cost Structure



WB BGA Package



FOWLP Package



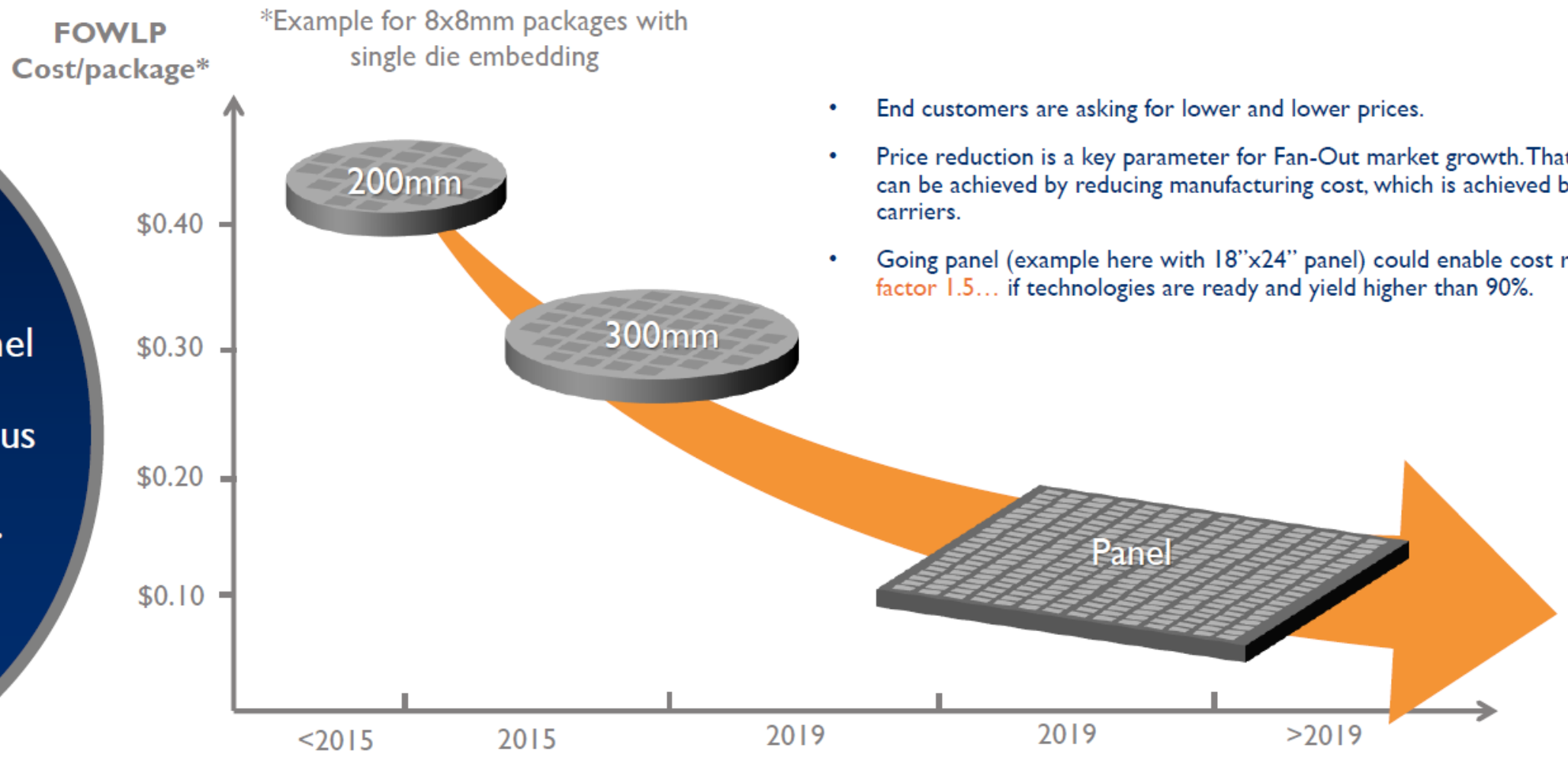
** For a reference scenario of 64 I/Os, 0.4mm pitch, same IC application*

- **BGA packaging technology has today reached a maturation point where it is difficult to scale the cost down further. On the other hand, FOWLP platform has a new value proposal because:**
  - **Substrate, Wire bonds, underfill and µ-bumps are removed → Reduced cost and no more substrate inventories!**
  - **The "BOM" – Bill Of Materials – is likely to aggressively scale down in cost with time, thanks to**
    - Standardization of new material selection (mold compound, passivation resists, chemistries & cleaners, etc.)
    - Amortization of the infrastructures (linked to new equipment introduced)
    - Combinations and synergy between Wafer Test/Final Test procedures

APPLIED MATERIALS

FOWLP Cost Analysis Conclusion

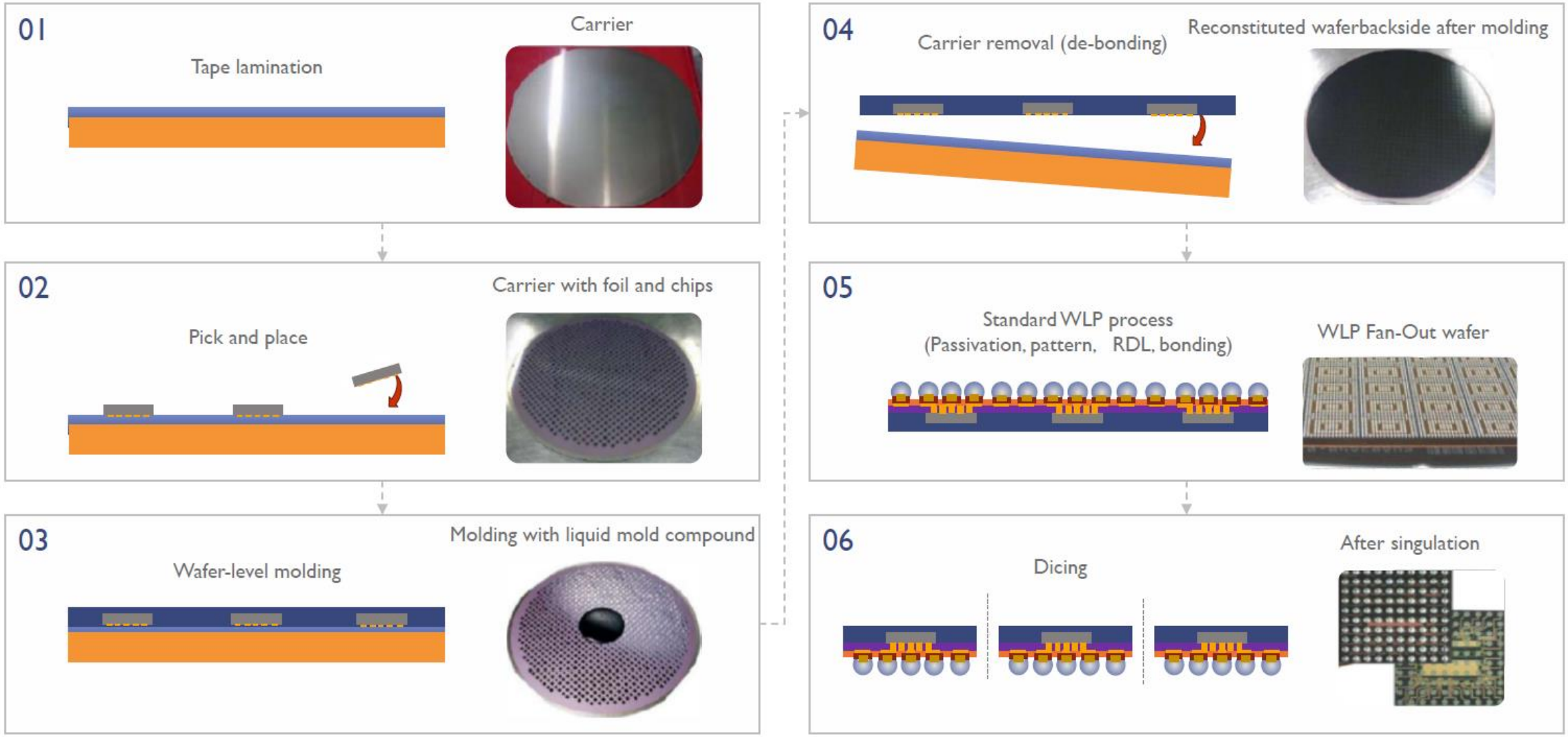
Going panel means tremendous cost reduction.



- End customers are asking for lower and lower prices.
- Price reduction is a key parameter for Fan-Out market growth. That price reduction can be achieved by reducing manufacturing cost, which is achieved by using larger carriers.
- Going panel (example here with 18"x24" panel) could enable cost reductions up to a factor 1.5… if technologies are ready and yield higher than 90%.

APPLIED MATERIALS

Fan-out packaging principle..



Fan-Out: Dies embedded in mold compound. No advanced substrate needed to fan out of chip surface.
eWLB example (chip-first face-down)

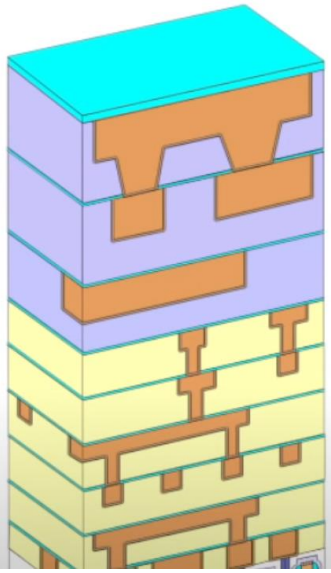
Source: Infineon

Reconstituted Wafer with the chip is subject to FEOL type processes…

Flip Chip BGA - uBumps

1

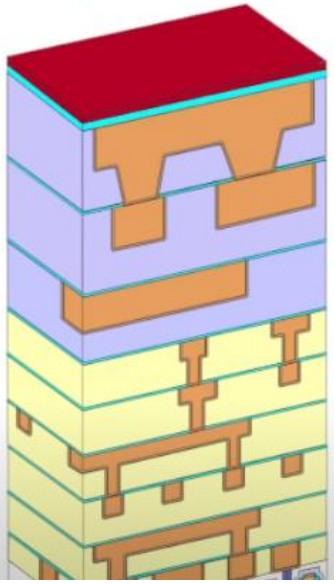
Final Passivation- Some combination of oxide and nitride put down by PECVD.



Flip Chip BGA - uBumps

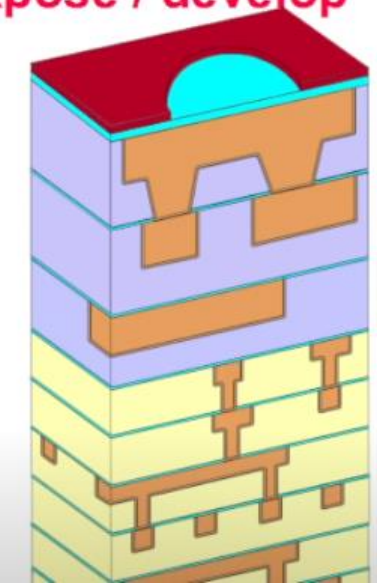
2

Spin on Photoresist



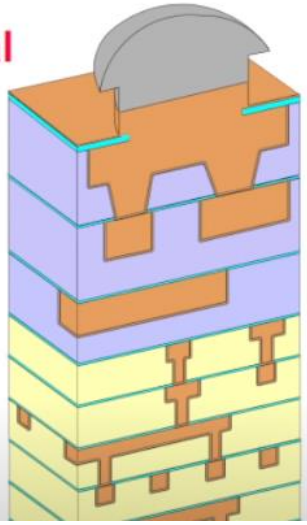
3

Expose / develop



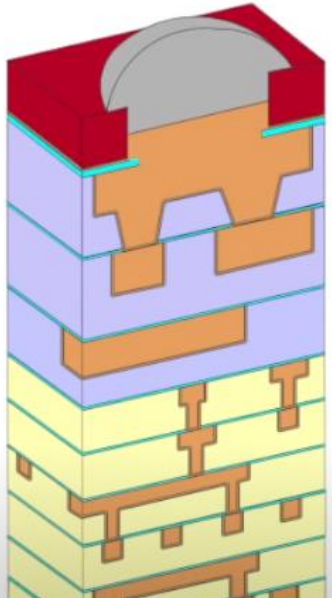
Solder bump Photoresist removal

6



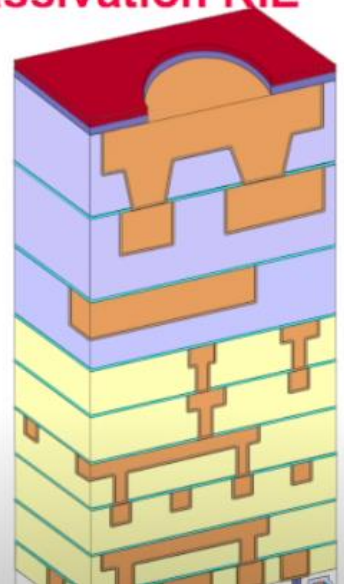
Solder bump Electrochemical deposition of solder

5



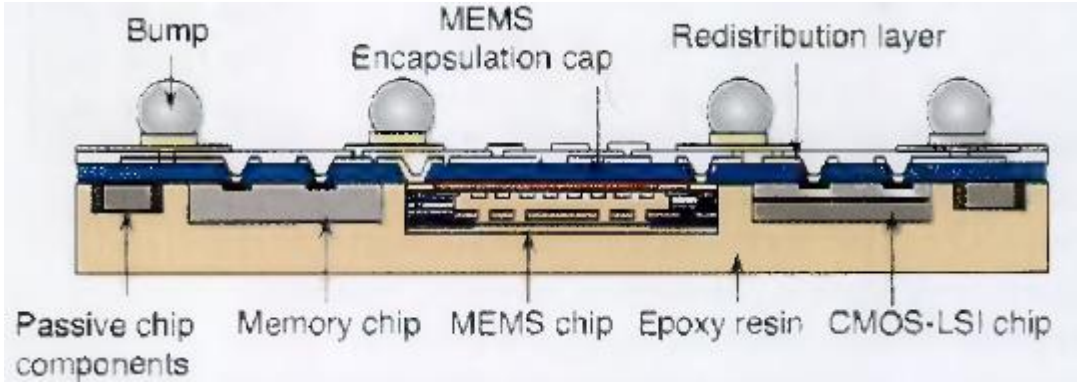
4

Passivation RIE

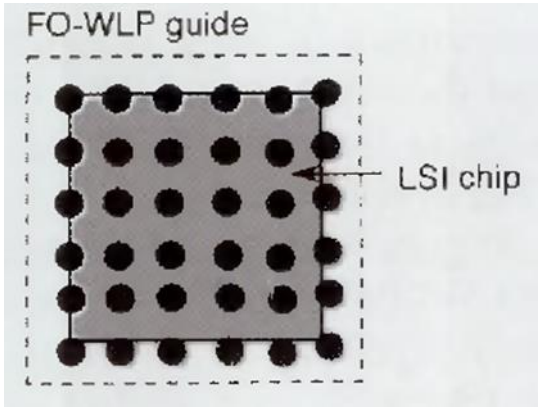
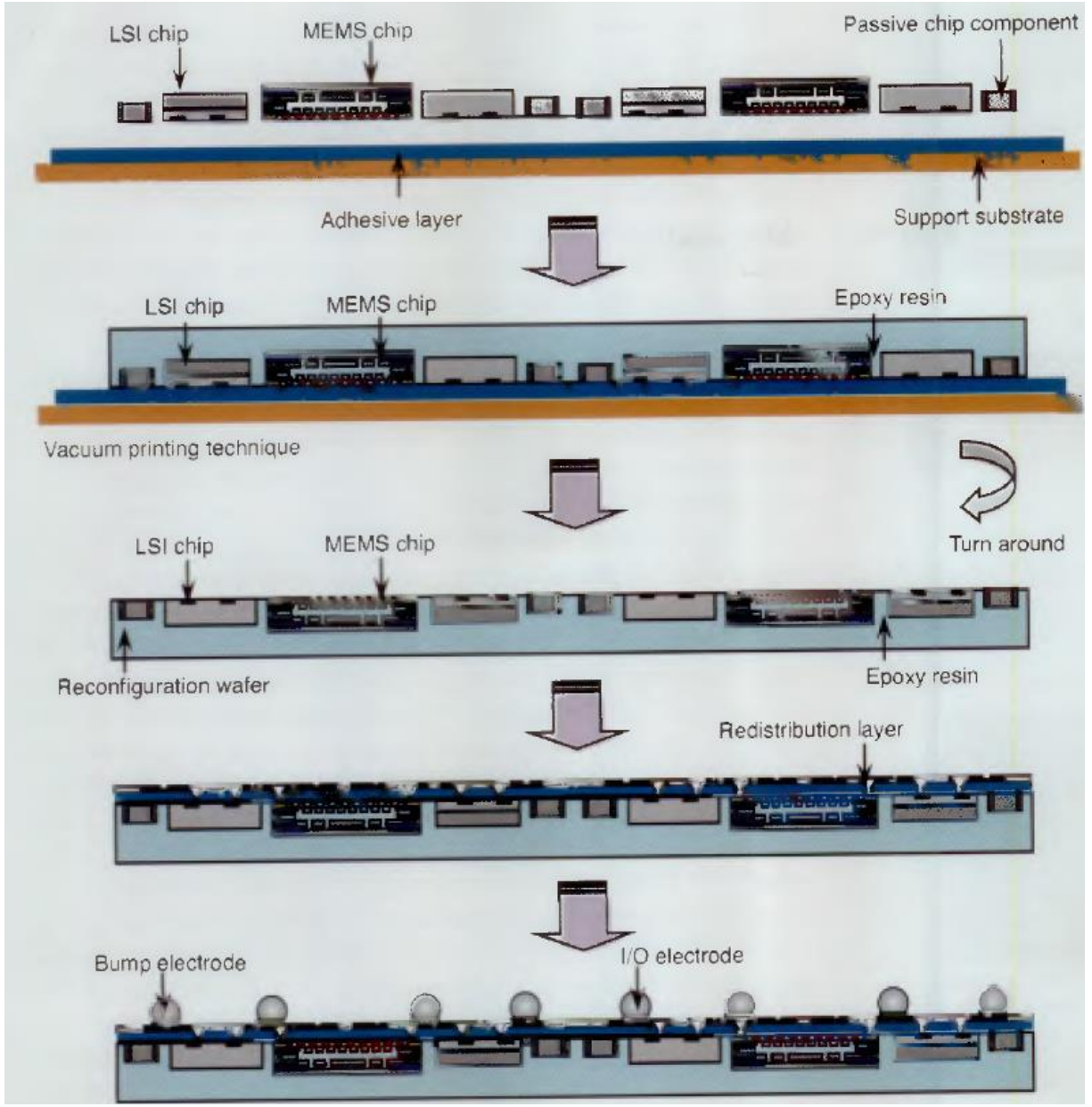


APPLIED MATERIALS

Fabrication Process: Multi-chip SoC (inFO)



Cross-sectional view of Multi-Chip-SoC



Source: AEI, Sept 2017