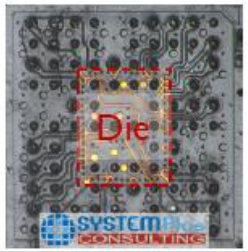
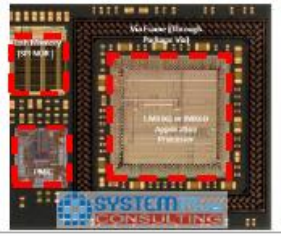
FAN-OUT TECHNOLOGIES: COST REVIEW

*Cost gap is wide within different types of Fan-Out Technologies

Technology	eWLB	ePLP		RCP			inFO
Schematic Overview *not drawn to scale*							
Schematic Cross-section *not drawn to scale*							
Package I/O Counts	~150	~500		~500			~1500
Carrier	FOWLP: 200mm	FOPLP: 415x510mm		FOWLP: 300mm			FOWLP: 300mm
RDL: L/S**	1xRDL: 18/39 um	3xRDL: 8/14 um		4xRDL: 14/60 um			3xRDL: 8/14 um
Die Count	Single-Die	Multi-Die		Multi-Die			Single-Die
Die Devices	RF	AP	PMIC	AP	PMIC	Memory	AP
Die Size	3x3 mm	5x4 mm	6x4 mm	7x7 mm	3x3 mm	4x4 mm	11x8 mm
Package Size	6x6 mm	9x8 mm		14x17 mm			15x15 mm
Market Application	Automotive: Radar	Consumer: Smartwatches		Computing: IoT			Mobile: Smartphones
*Cost/Die Area	$0.045/mm^2	$0.017/mm^2		$0.025/mm^2			$0.020/mm^2

FAN-OUT PACKAGING SUPPLY-CHAIN: POSITIONING OF OSATS

*OSATs are well-established in Core Fan-Out market and naturally position themselves from low-end to mid-end market.

JCET, Deca Technologies, Amkor Technology, nanium, nepes, ASE GROUP → Pioneers to enter market and now leading it with volume.

Powertech Technology Inc., ASE GROUP, Deca Technologies, nepes → FOPLP to reduce cost. PTI first in production. Attracts fabless.

Amkor Technology, SPIL → Develop FO technology recently but limited customer traction.

3plus, AURORA SEMICONDUCTOR → Focus on specialized market and small series

OSATs | IDMs | Foundries

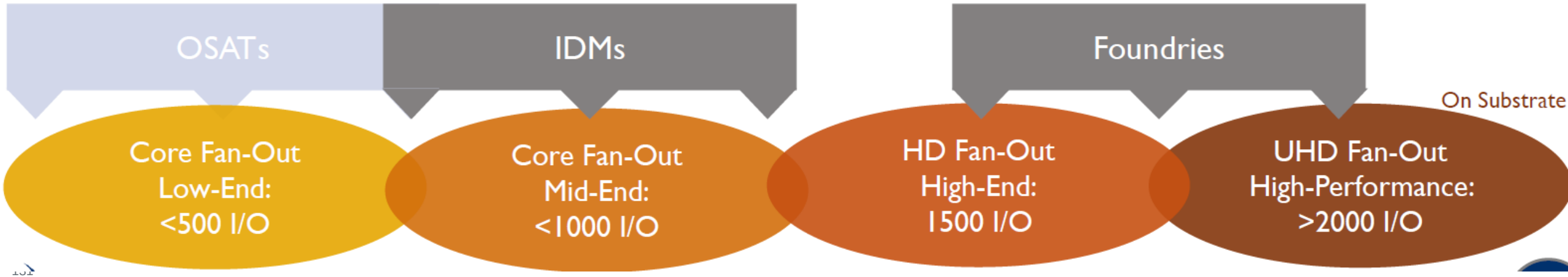
On Substrate

- Core Fan-Out Low-End: <500 I/O
- Core Fan-Out Mid-End: <1000 I/O
- HD Fan-Out High-End: 1500 I/O
- UHD Fan-Out High-Performance: >2000 I/O

FAN-OUT PACKAGING SUPPLY-CHAIN: POSITIONING OF IDMS/FOUNDRIES

*Foundries/IDMs are pushing for own FO technologies with different market positioning due to strategic or political reasons.

tsmc	First to enable HD FO for iPhone's APE . Target higher-end HPC next.
SAMSUNG / SAMSUNG ELECTRO-MECHANICS	First to enable FOPLP with APE/PMIC for galaxy watch (consumer).
Infineon / NXP / freescale semiconductor	Developed FOWLP technologies and has been licensing it.
ST life.augmented / GLOBALFOUNDRIES	Collaborating with OSATs & R&D institutes to assess FO capability



FAN-OUT APPLICATIONS

Where do we find Fan-Out? Some examples below

Orange: Devices that can be found in FOWLP packages today

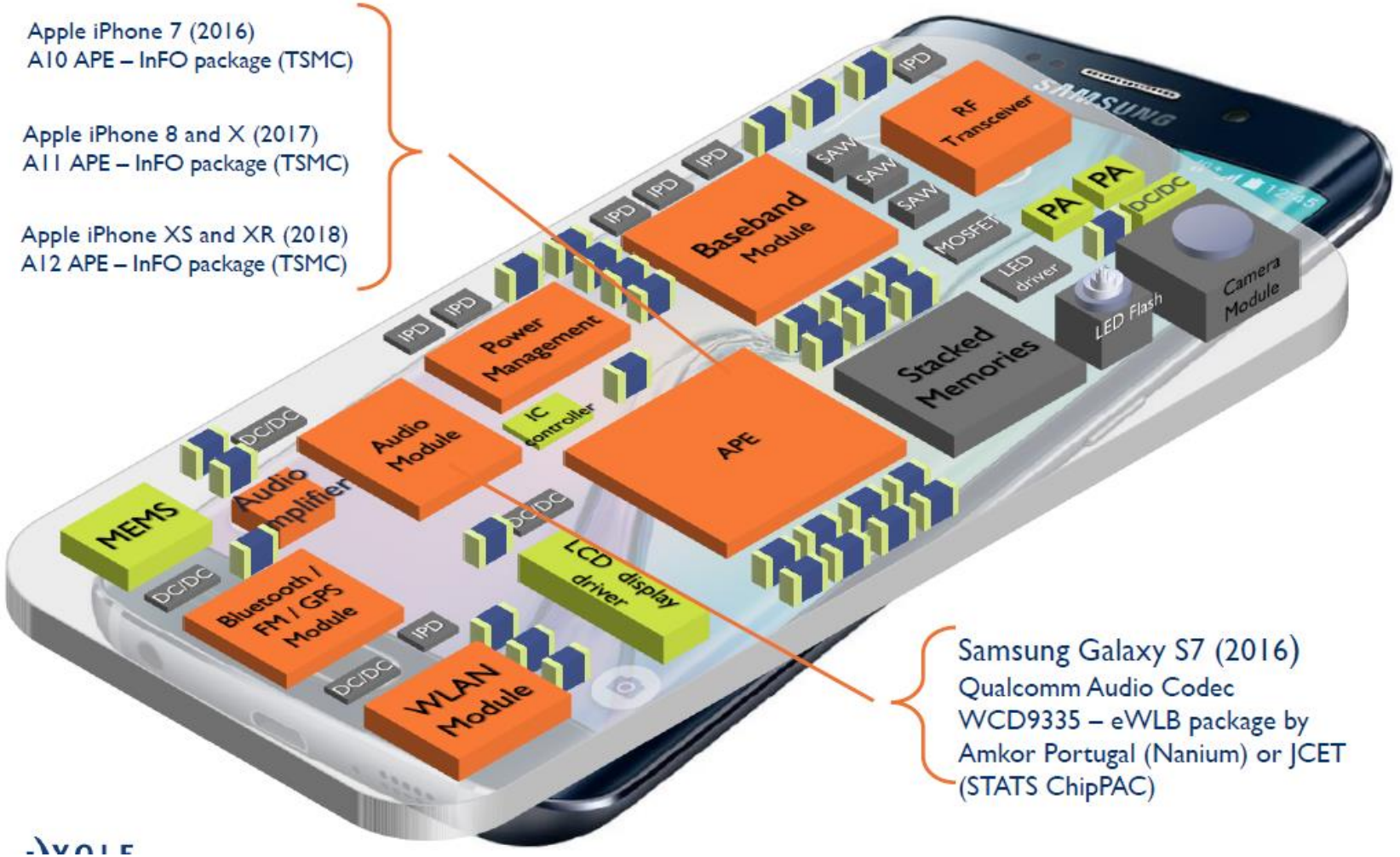
Green: Devices that could be found in the future in FOWLP

Grey: Devices that will likely remain on WLCSP or flip-chip package or move to 3DIC or Embedded die

Apple iPhone 7 (2016)
A10 APE – InFO package (TSMC)

Apple iPhone 8 and X (2017)
A11 APE – InFO package (TSMC)

Apple iPhone XS and XR (2018)
A12 APE – InFO package (TSMC)



Samsung Galaxy S7 (2016)
Qualcomm Audio Codec WCD9335 – eWLB package by Amkor Portugal (Nanium) or JCET (STATS ChipPAC)

Applications out of mobile market

Bosch MRR1Plus Radar (2015)
Infineon RASIC™ (77GHz RADAR System IC Chipset) – eWLB Package

Continental ARS400 Radar (2015)
NXP MR2001 (77GHz multichannel RADAR) – RCP Package

BK Ultrasound Sonic Window (2015)
Multichip Module – eWLB Package Amkor Portugal (Nanium)

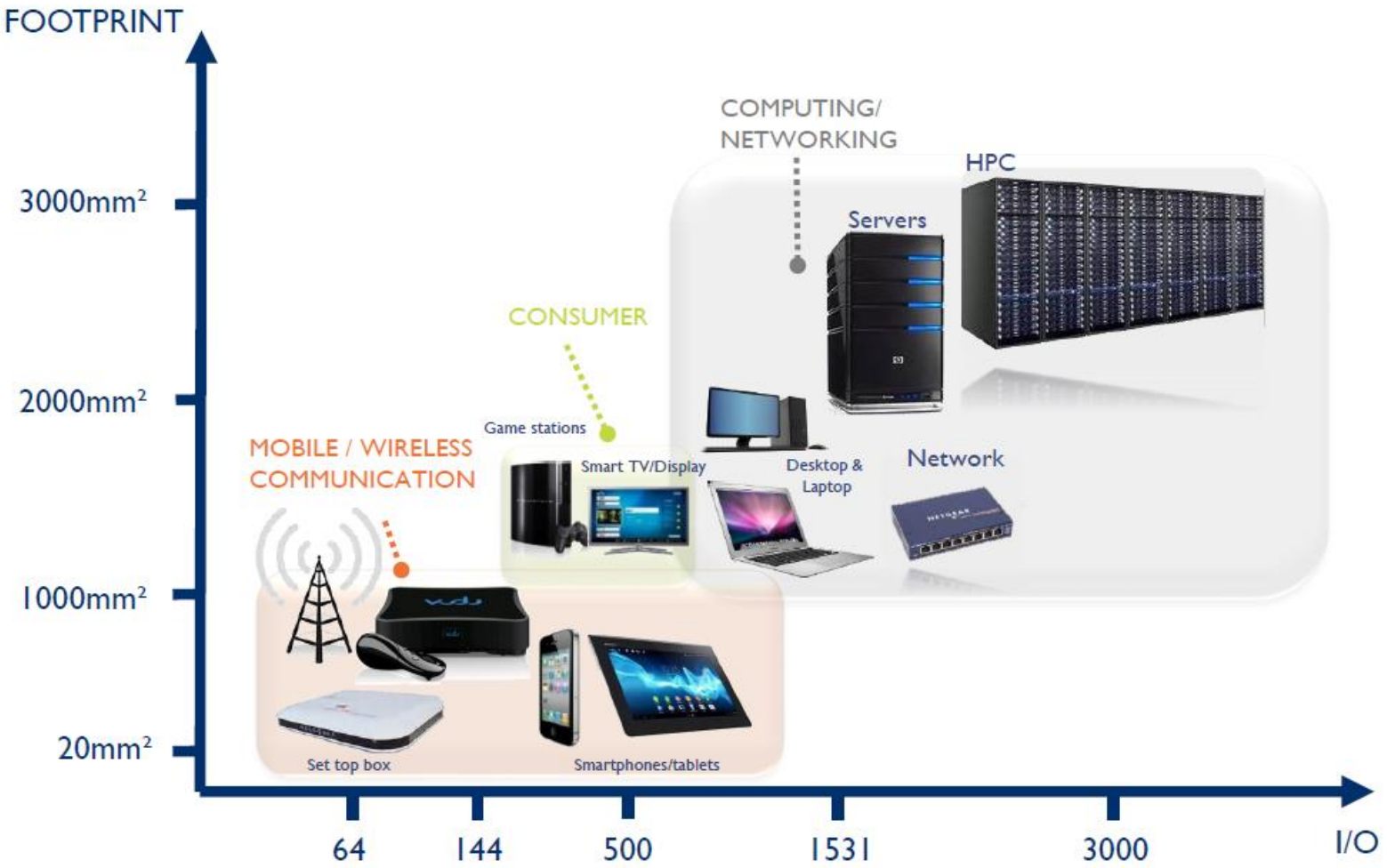
NXP SCM-iMX6Q (2017)
APE, PMIC and Flash memory – Fan-Out PoP (Nepes)

Samsung Exynos 9110 ePLP (2018)
APE, PMIC– FOPLP (SEMCO)

WHERE ARE ADVANCED PACKAGES FOUND TODAY?

2017

Fan-Out WLP volume is currently limited to mobile (SPs, tablets), while FC CSP/BGA spans all advanced markets

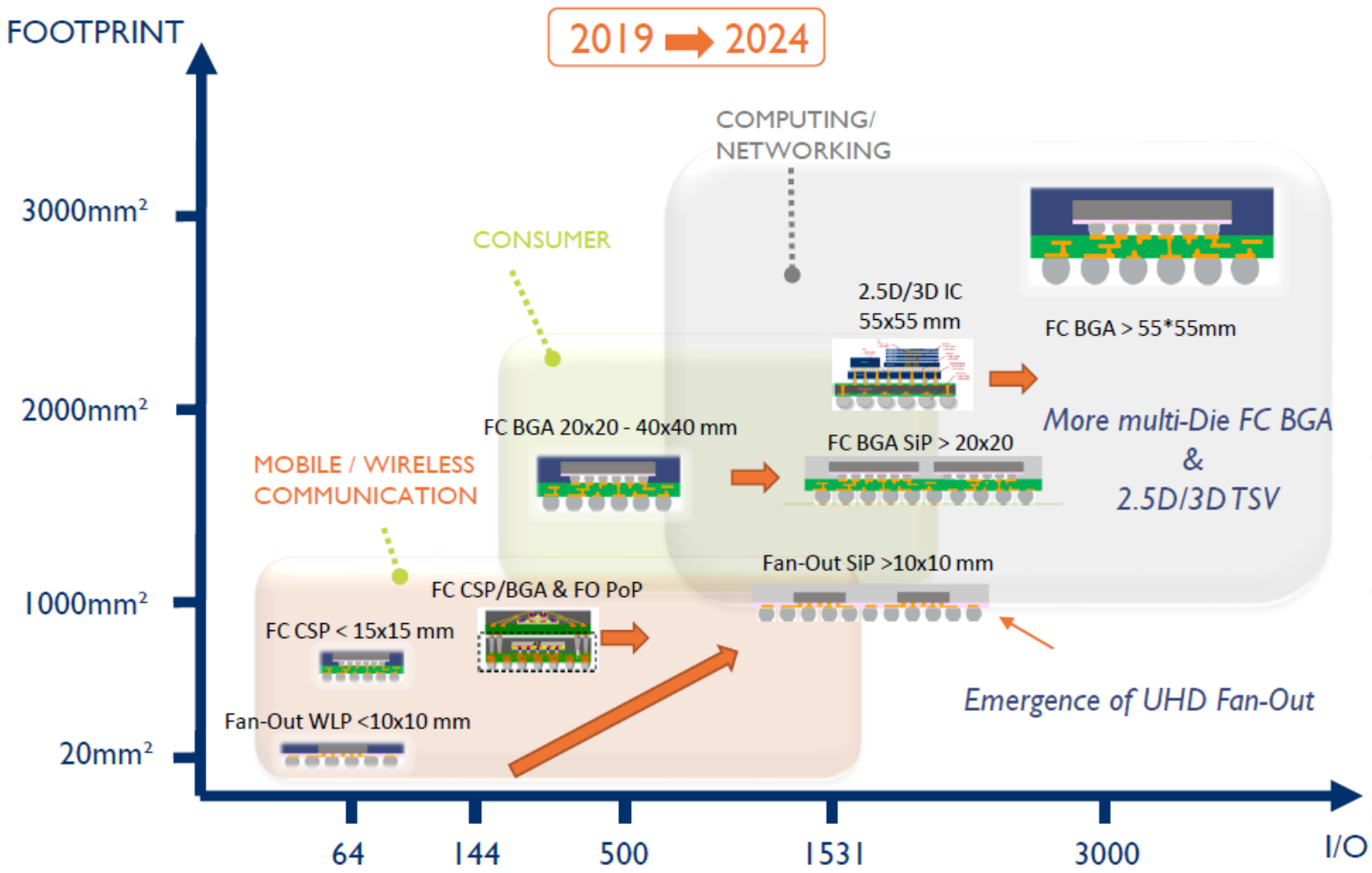


- Fan-Out WLP have exhibited high growth in smartphones and tablets, but have seen limited adoption outside of the mobile segment
- FC CSP/BGA is the most widespread advanced packaging platform found in all advanced markets

FLIP CHIP AND FAN OUT PACKAGING – 2019 TO 2024

Low cost, high resolution multi-die solutions

Further scaling below L/S < 10/10 um and more multi-die solutions (SiP/SiM)!

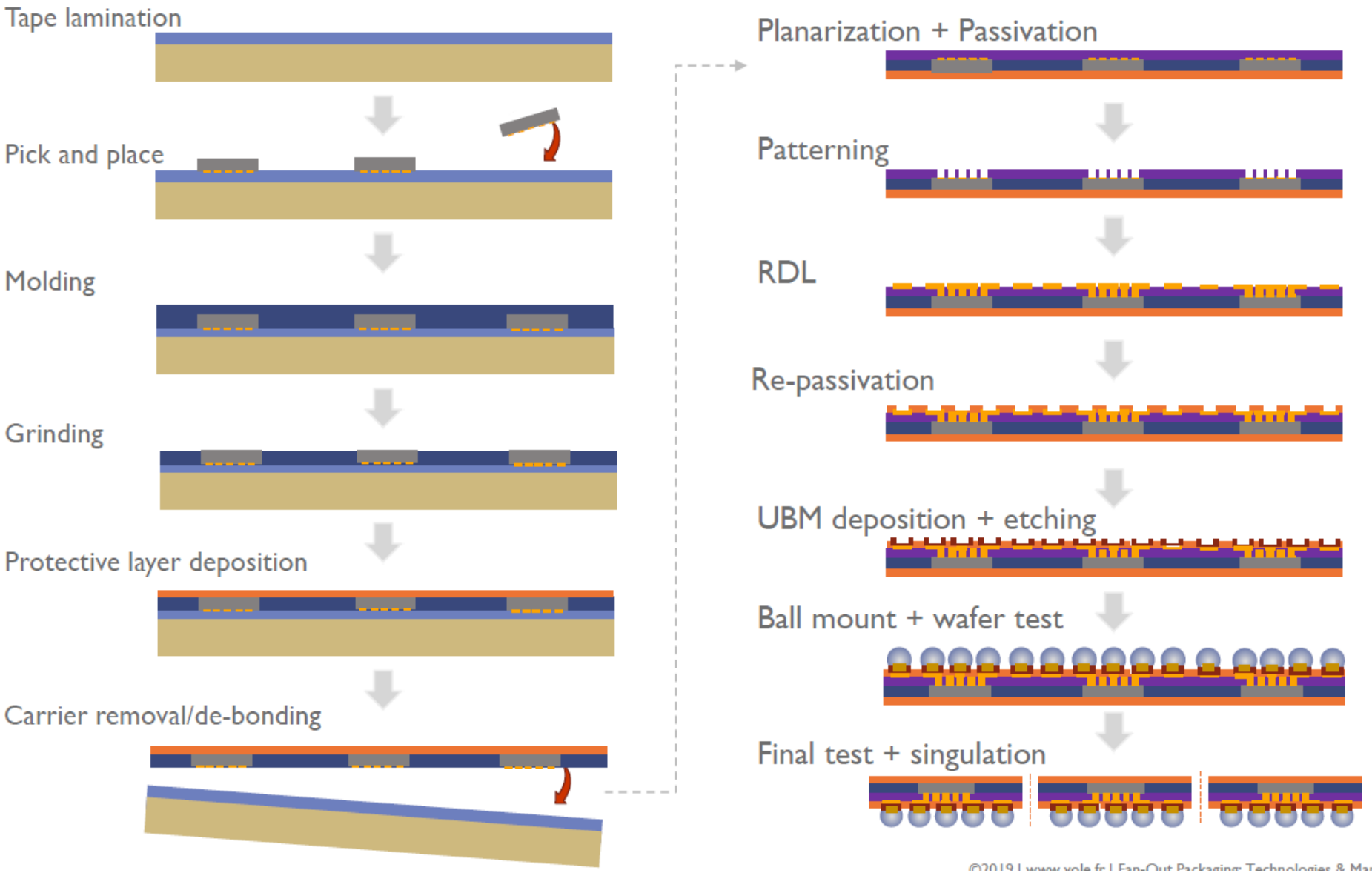


- Further development of Fan-Out WLP will bring high-density solutions and larger Fan-Out packages, single and multi-die that will further spread into computing / networking and high end consumer markets, attempting to offer lower cost and similar or potentially higher performance than FC BGA and 2.5D/3D IC solutions
- More commercialization of 2.5D/3D IC
- More multi-die solutions in conventional advanced FC and hybrid FC and Fan-Out packaging
- Largest FC BGA (~ >40x40 mm) are likely to be still out of reach for Fan-Out solutions

CHIP-FIRST FACE-DOWN

eWLB process example

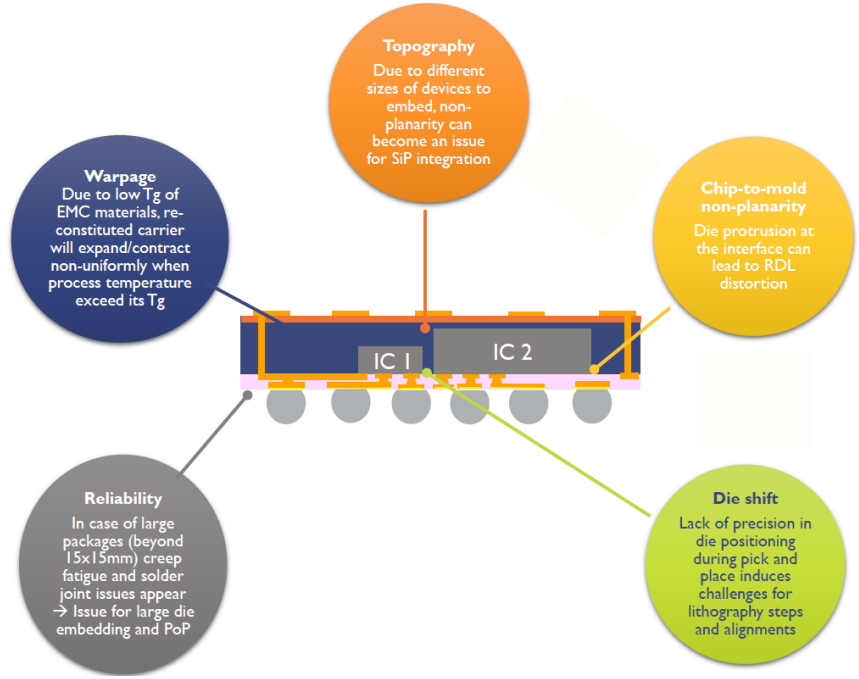
Full Chip-First Face-Down process example.



FOWLP Overall Conclusions

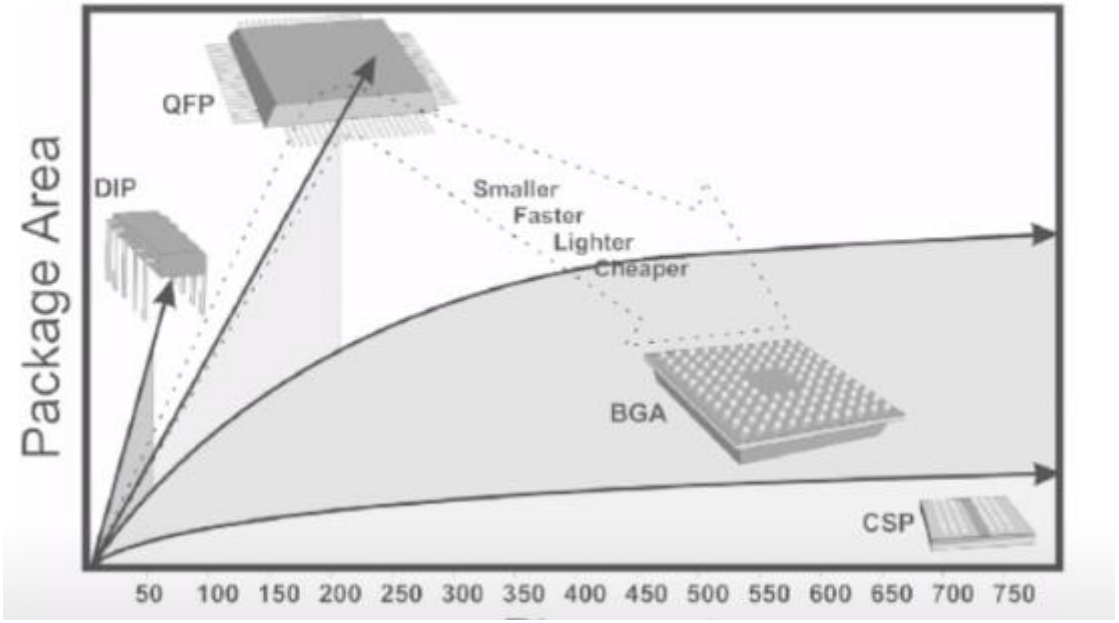
- FOWLP is now a mainstream packaging platform with all key OSATs, IDMs and Foundries – offering breakthru integration & miniaturization (5um line/space, reduced package thickness< 0.5mm etc)
- FOWLP extends the concept of wafer scale packaging to many new applications that are packaged in BGA& WL CSP packages
- Key applications driving FOWLP volume demand will be wireless basebands, RF transceivers, Power management Units. Other applications include stacked memories, anolog-specific Ics such as audio-codec, MEMS & Sensors, network switches etc
- Further opportunity to scale packaging cost down by:
  - Increasing wafer diameter (300mm) and moving to panel size (PLP sees emergence of SEMTECH and PTI)
  - Decreasing importance of material colume in general as substrate is removed
  - Simplifying the manufacturing infrastructure

Fan-Out packaging faces technical challenges it must overcome to enlarge its scope of compatible applications.



Packaging – Overall Conclusions

- Evolving and tech intensive
- Driven by:
  - Increasing # of interconnects
  - Lowering cost/interconnect
  - And…now
  - Improving functionalities in
    - Power
    - Performance
    - Bandwidth
    - And Sector Specific Utilization…
  - Future will have exciting evolution with
    - Chiplets (CHIPS program)
    - SiP with added functionalities from Heterogenous Integration…and More!



Overview of Applied Materials Advanced Packaging Capabilities

External Use

Applied Materials Global R&D Infrastructure

Maydan Technology Center (MTC)

LOCATED IN SANTA CLARA, CA

39K SQFT CLASS 1 CLEANROOM: 120 tools
The most comprehensive suite of the 300mm wafer fabrication equipment in WFE industry

HEADQUARTERS, MAIN R&D LAB: Product development transistors, interconnects, memory applications

Asia Product Development Center (APDC)

LOCATED IN SINGAPORE: Dedicated advanced packaging center since April 2012

17K SQFT CLASS 10 CLEANROOM:
11 Applied platforms & over 40 supporting tools

> 70 STAFF: Product/hardware development, process integration, test vehicle design & electrical-testing, customer demos for WLP-TSV

APPLIED MATERIALS

Applied Packaging Development Center

Adding Value Leveraging Our Advanced Packaging Capability

Singapore | 17k Sqft Cleanroom | >70 Employees

11 Applied Platforms • 40 Supporting Tools ● +24 New Tools

WLP, Cu Pillar/Bump, Fan-out & TSV

Materials Innovation to enable Packaging Technology

Develop High Performance & Cost Competitive Products for WLCSP. Products include PVD,ECD, UBM Etch, PR strip & Defect Review

Identify and Solve Customer High Value Problems for Packaging Development and High Volume Manufacturing

APPLIED MATERIALS

Applied Materials' Products for Bump, RDL, Fanout

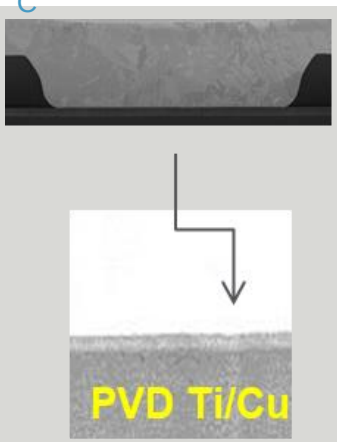
Charger PVD

Nokota ECD

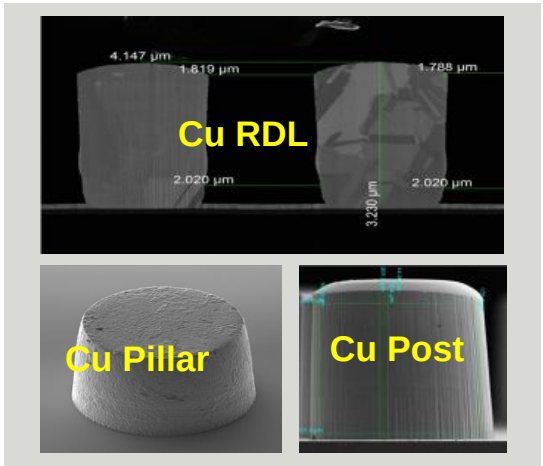
Raider UBM Etch

Reflexion LK CMP

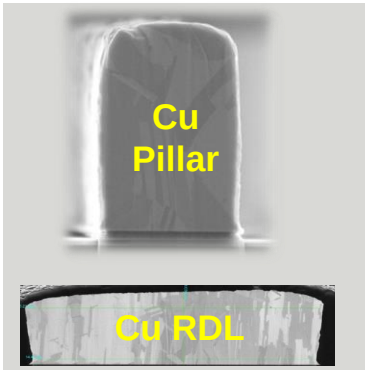
Low-R_C PVD UBM / RDL



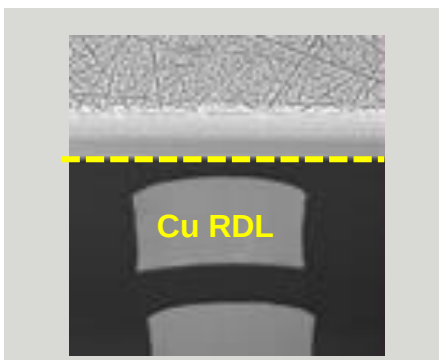
ECD solder / RDL / Pillar / Post



UBM Etch



Polymer CMP



APPLIED MATERIALS

Applied Materials' Products for TSV Creation/BVR

APPLIED MATERIALS®

Key Messages

- Advanced Packaging seeing an evolution of Middle End-of-line processes
- The MEOL processes are driving increased I/O per die, at lowered costs – both Opex and leveraged Capex, enhanced functionalities
- Process recipes are customized to individual end-device
- …and for specific end-sector applications
- Devices are getting designed with advanced EDA tools – it is not a guess-ware
- Given a process recipe from a technology provider, industrial engineers/consultants will define the factory equipment by selecting the appropriate tools as per the output mix . In most cases, the technology provider will give the factory equipment list to enable proven yield (and demand)
- Sector/Industry specific standards are shaping out to evolve the heterogenous integration

APPLIED MATERIALS®